

MS-7245 (Babel)

Version 0B

System Chipset:

Intel Broadwater - GMCH (North Bridge)

Intel ICH8(DO) (South Bridge)

On Board Chipset:

BIOS -- SPI Flash 8Mb or 16Mb

HD AUDIO -- ALC262

LPC Super I/O -- SMSC--SHC5017

LAN -- Intel Neneveh 82566

IDE-- VIA VT-6410

CLOCK -- ICSLP505-1

Main Memory:

2 CHANNEL DDR II * 4 (Max 8GB)

Expansion Slots:

PCIE x16 SLOT * 1

PCIE x1 SLOT * 1

PCI SLOT * 1

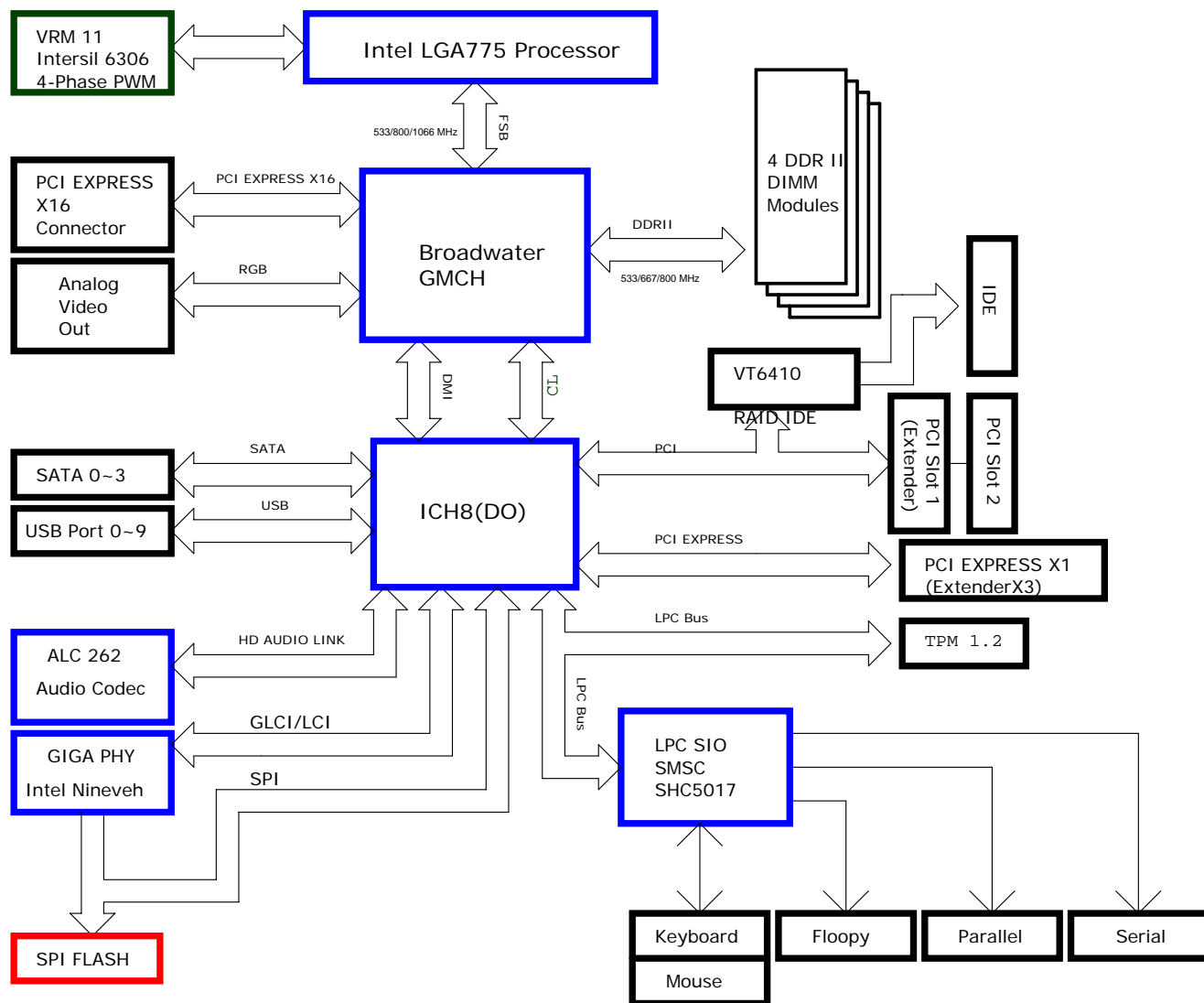
PCI Extender SLOT * 1

Intersil PWM:

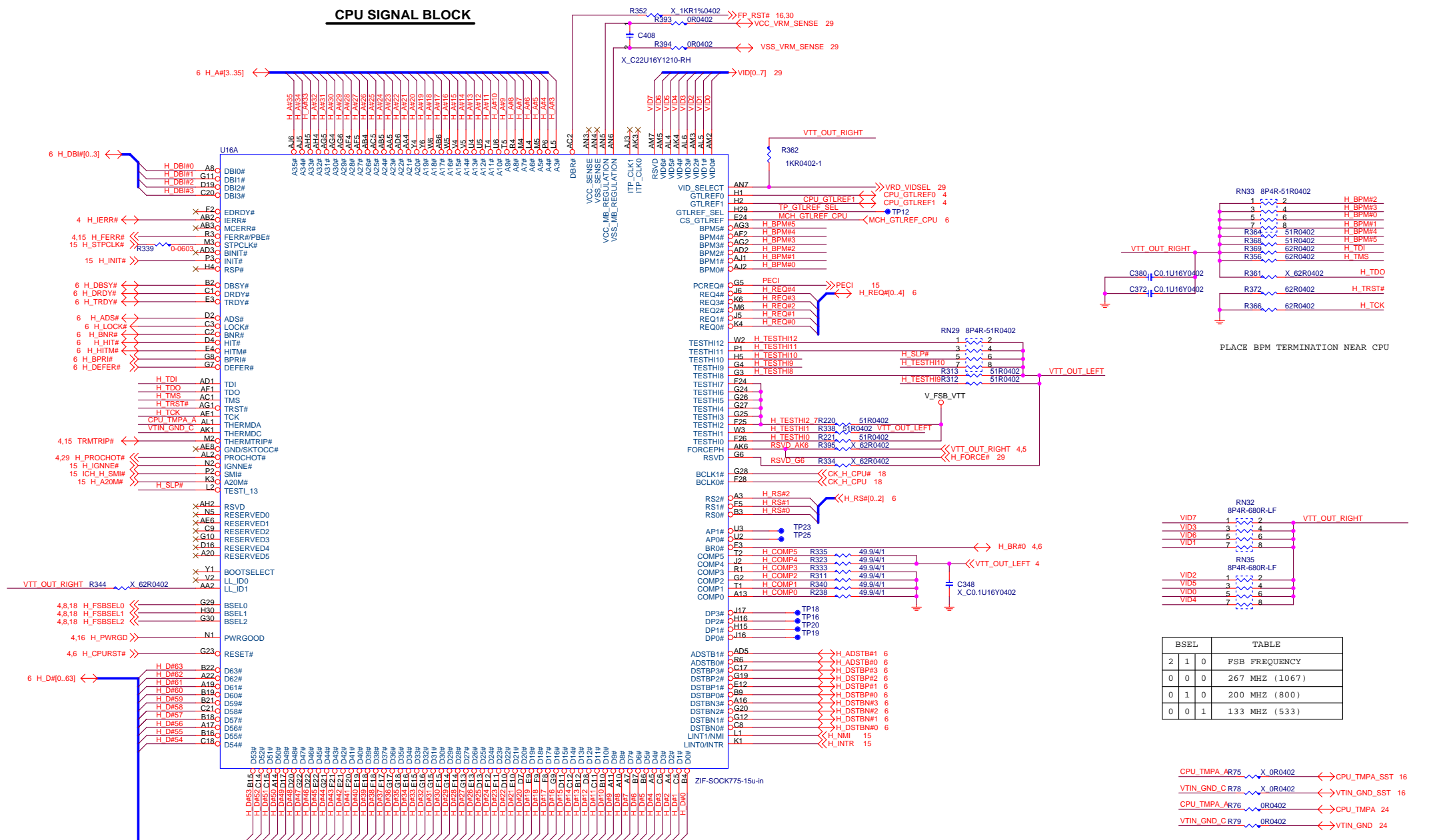
Controller: INTERSIL 6306 4 PHASES

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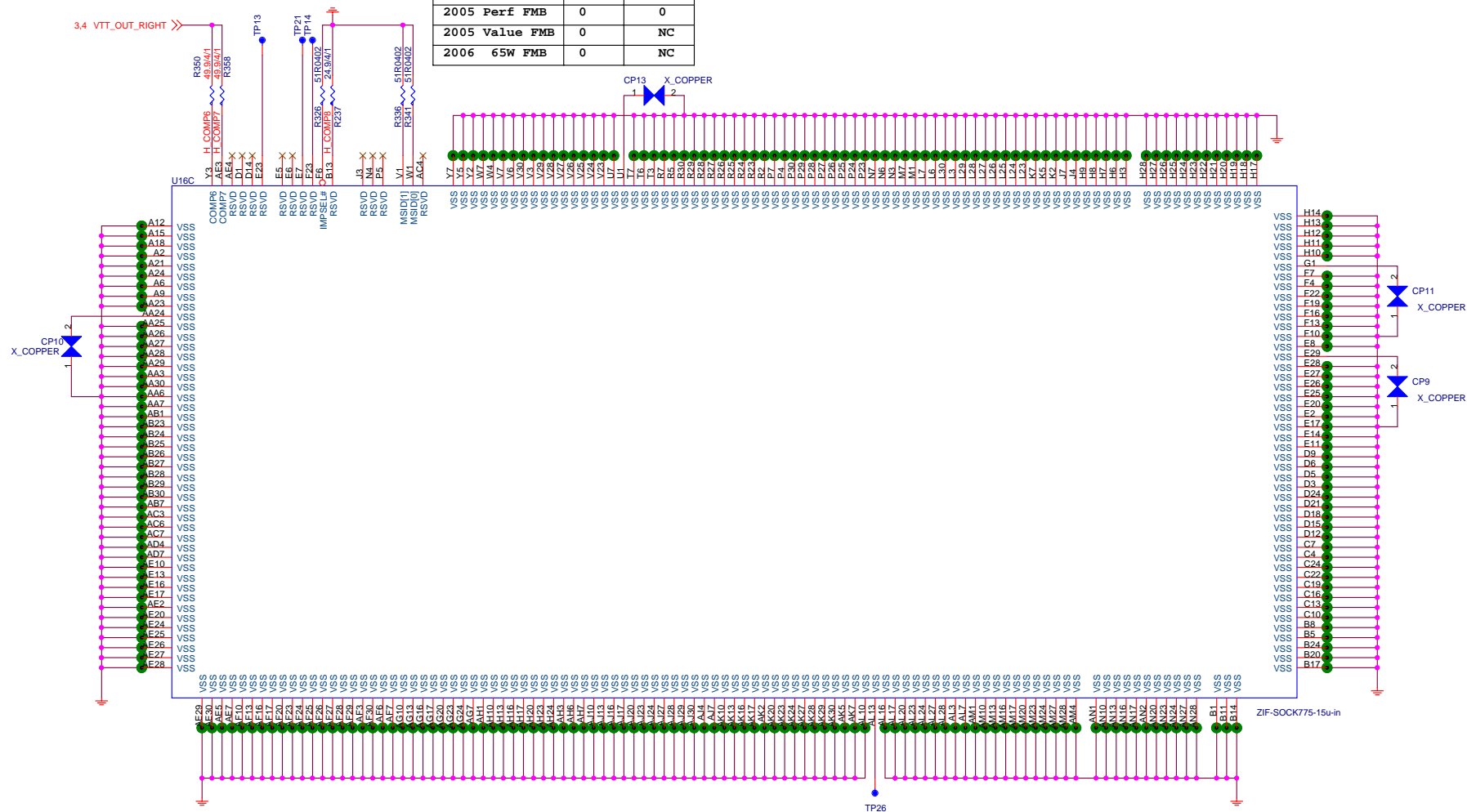
Block Diagram



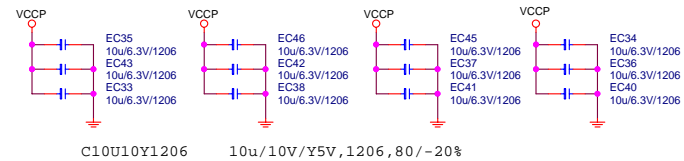
CPU SIGNAL BLOCK



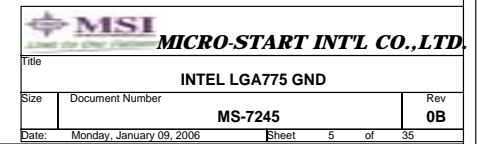
	MSID1	MSID0
2005 Perf FMB	0	0
2005 Value FMB	0	NC
2006 65W FMB	0	NC

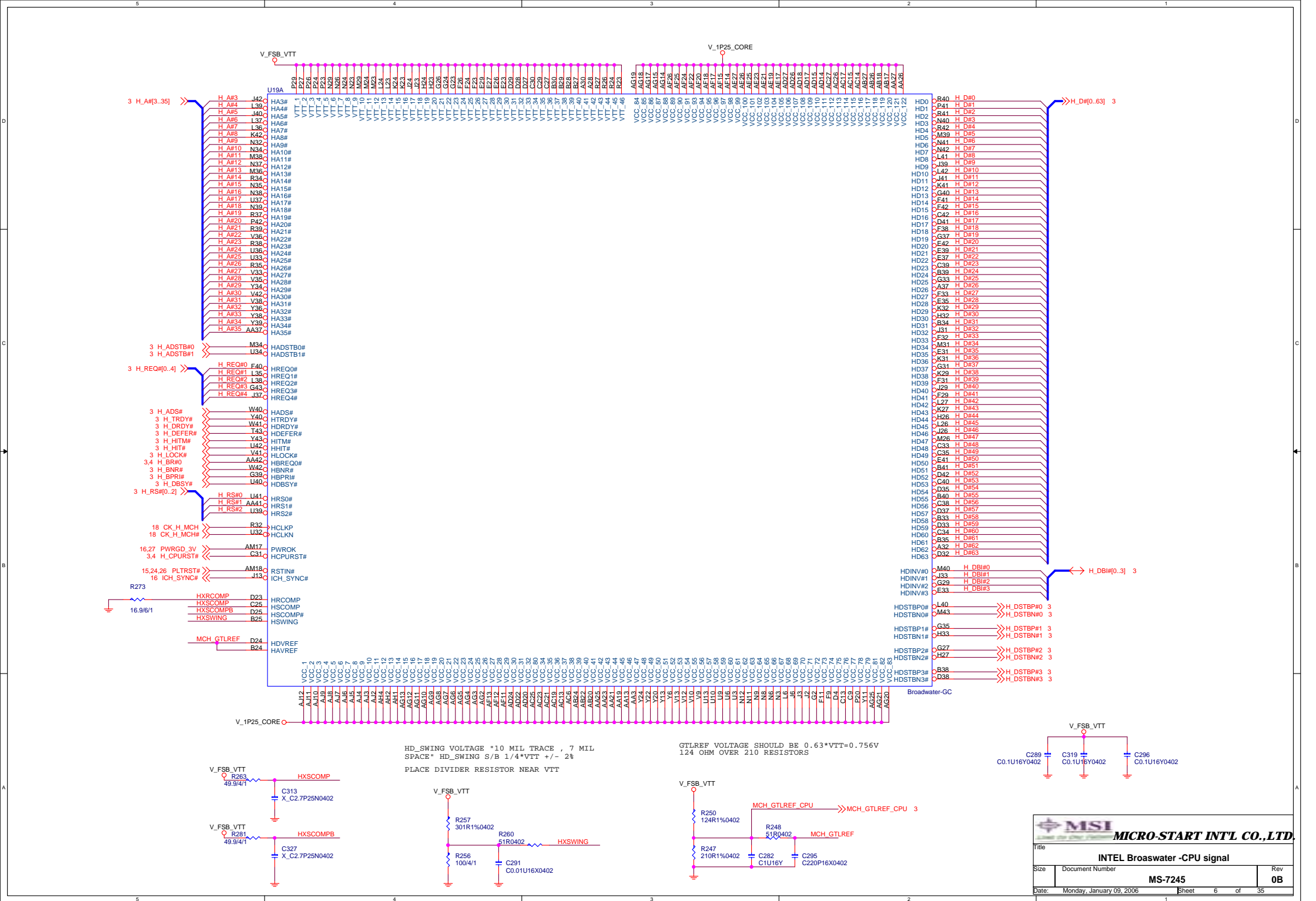


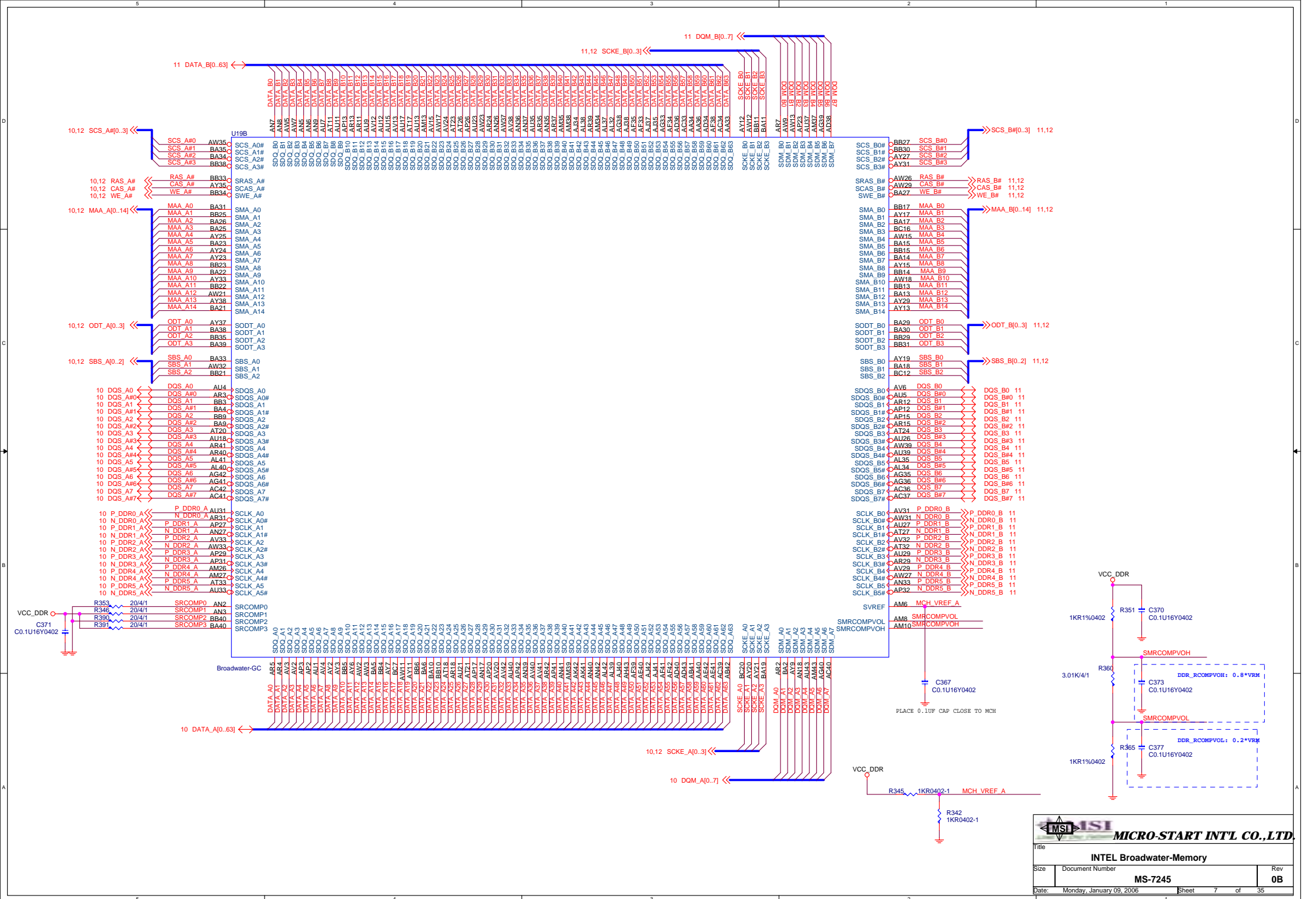
CPU DECOUPLING CAPACITORS

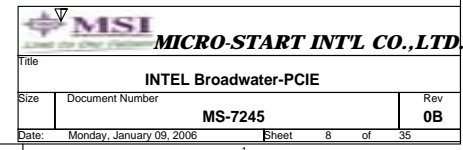


Place these caps within socket cavity



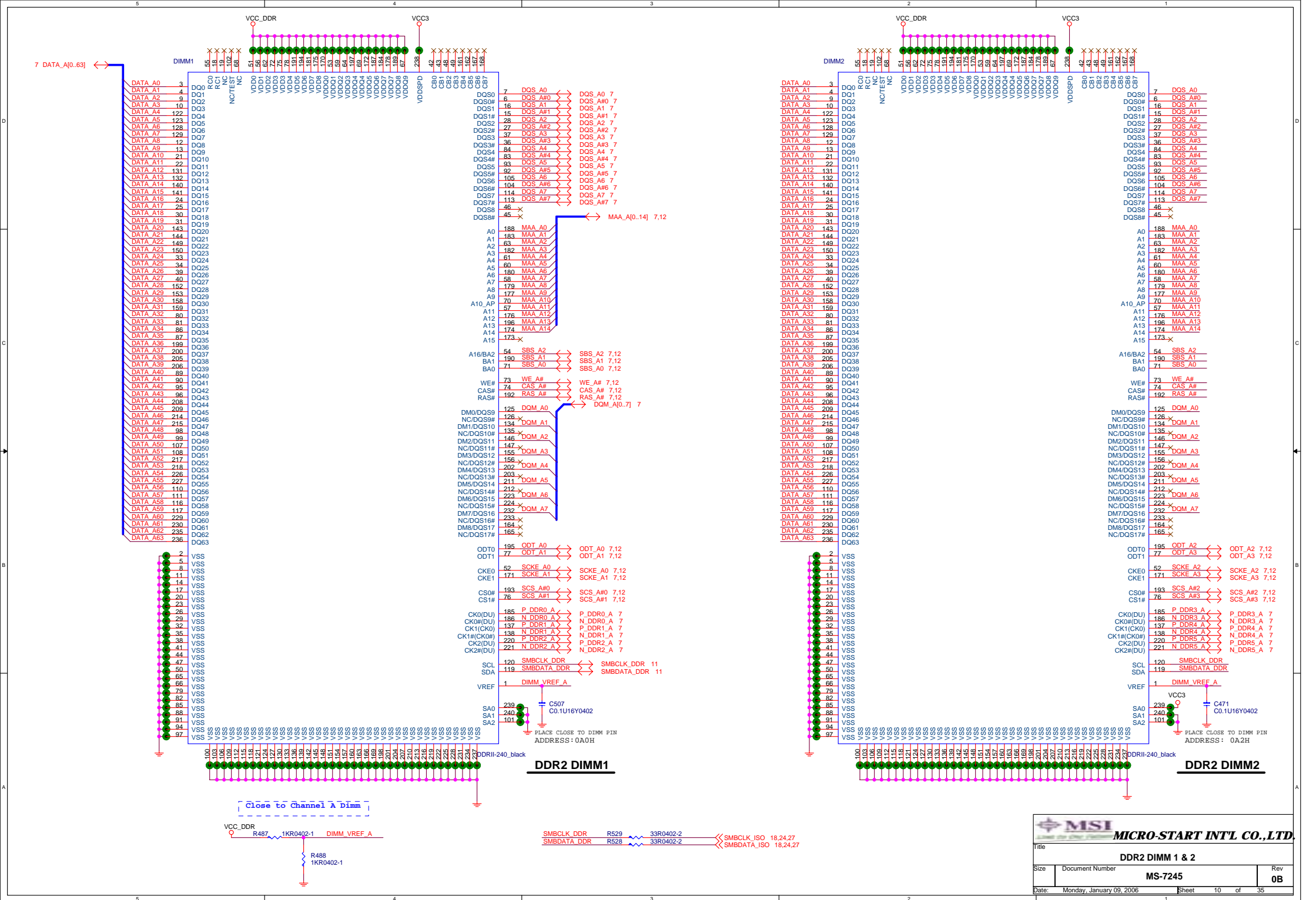






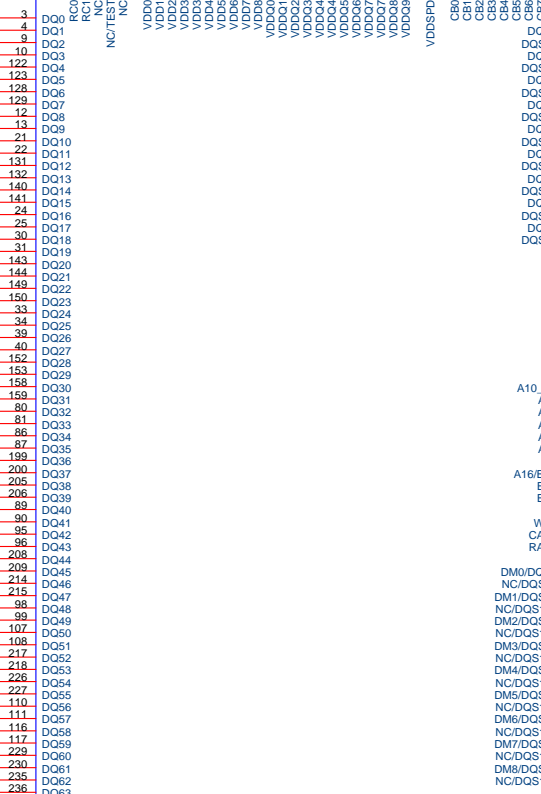
V_1P25_CORE



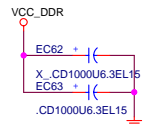
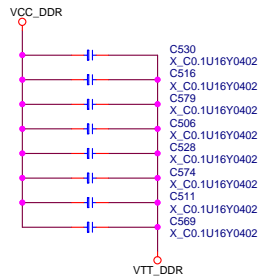
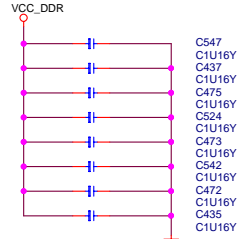
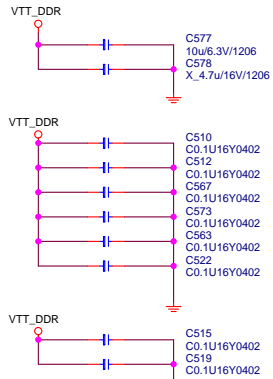


7 DATA_B[0..63]

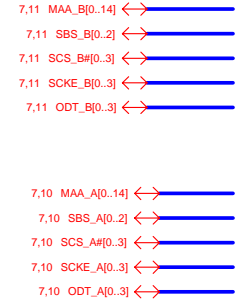
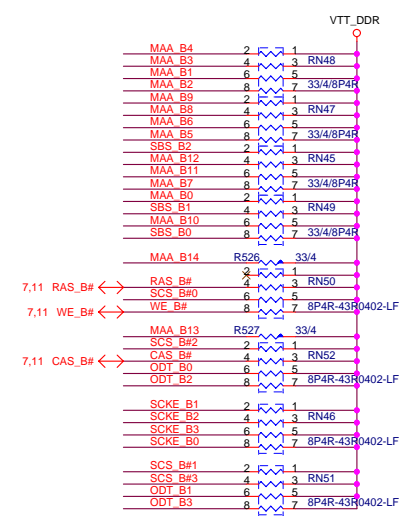
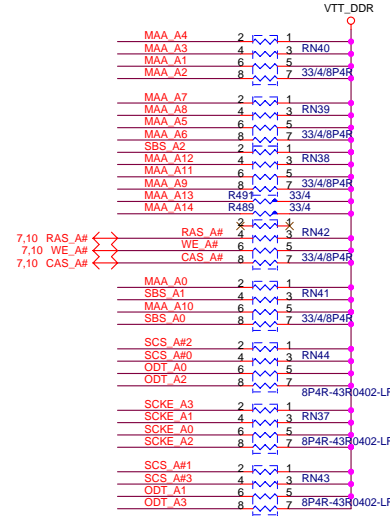
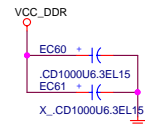
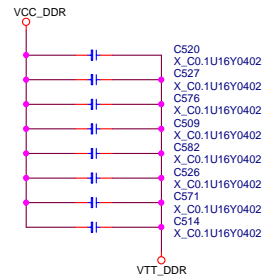
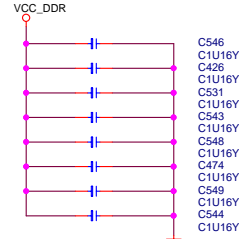
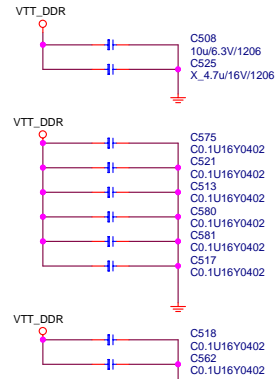
DIMM3



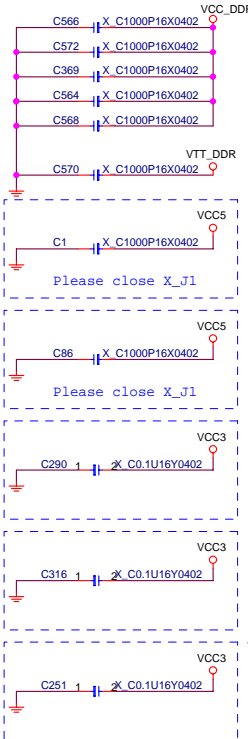
CHANNEL A V_SM_VTT DECOUPLING CAPS



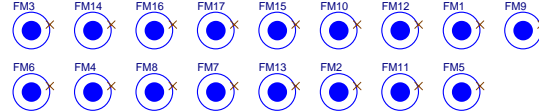
CHANNEL B V_SM_VTT DECOUPLING CAPS



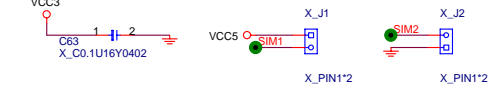
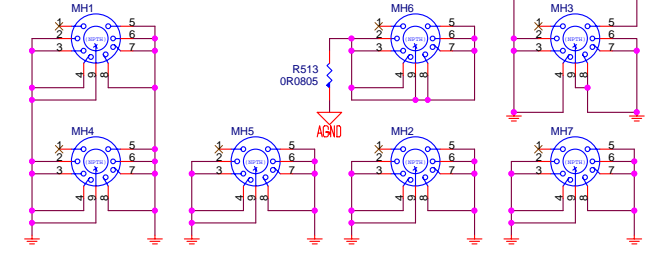
EMI CAPS reserve



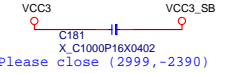
Optical Fiducial Marks



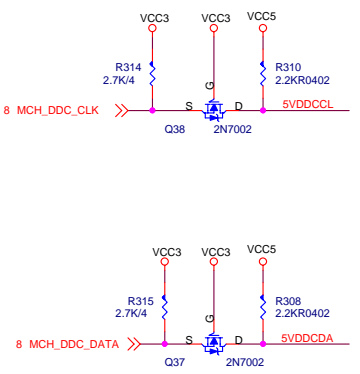
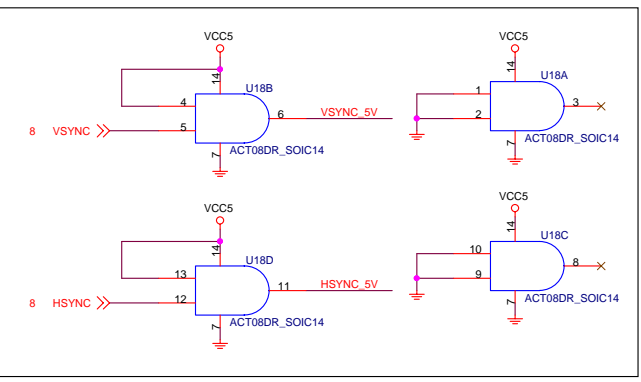
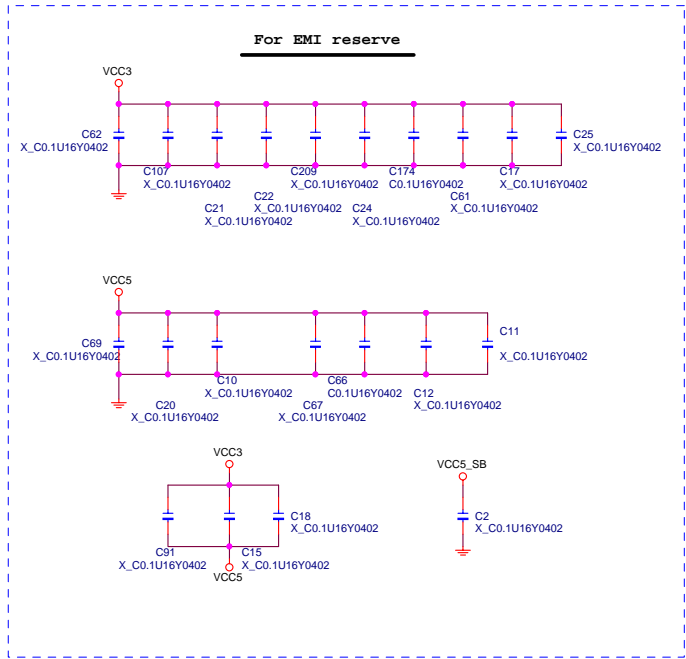
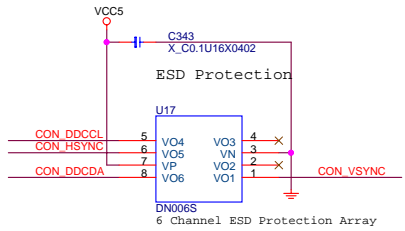
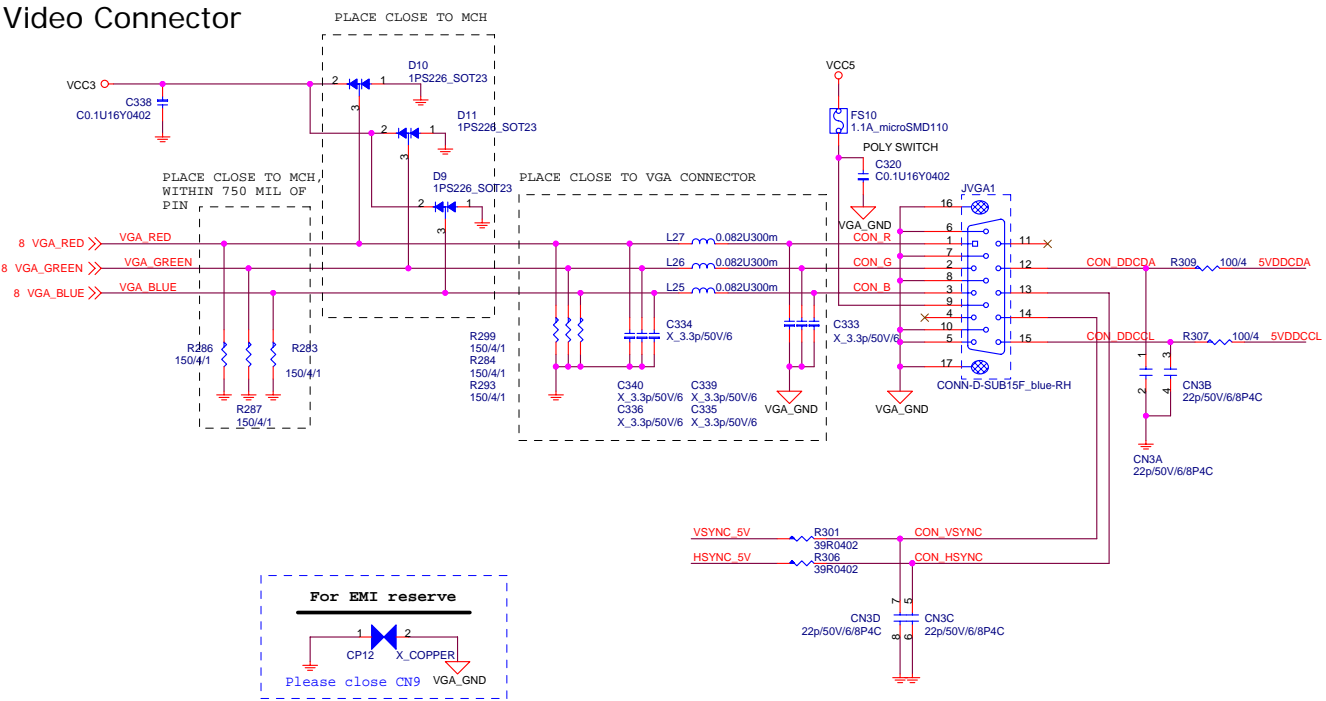
Mounting Holes




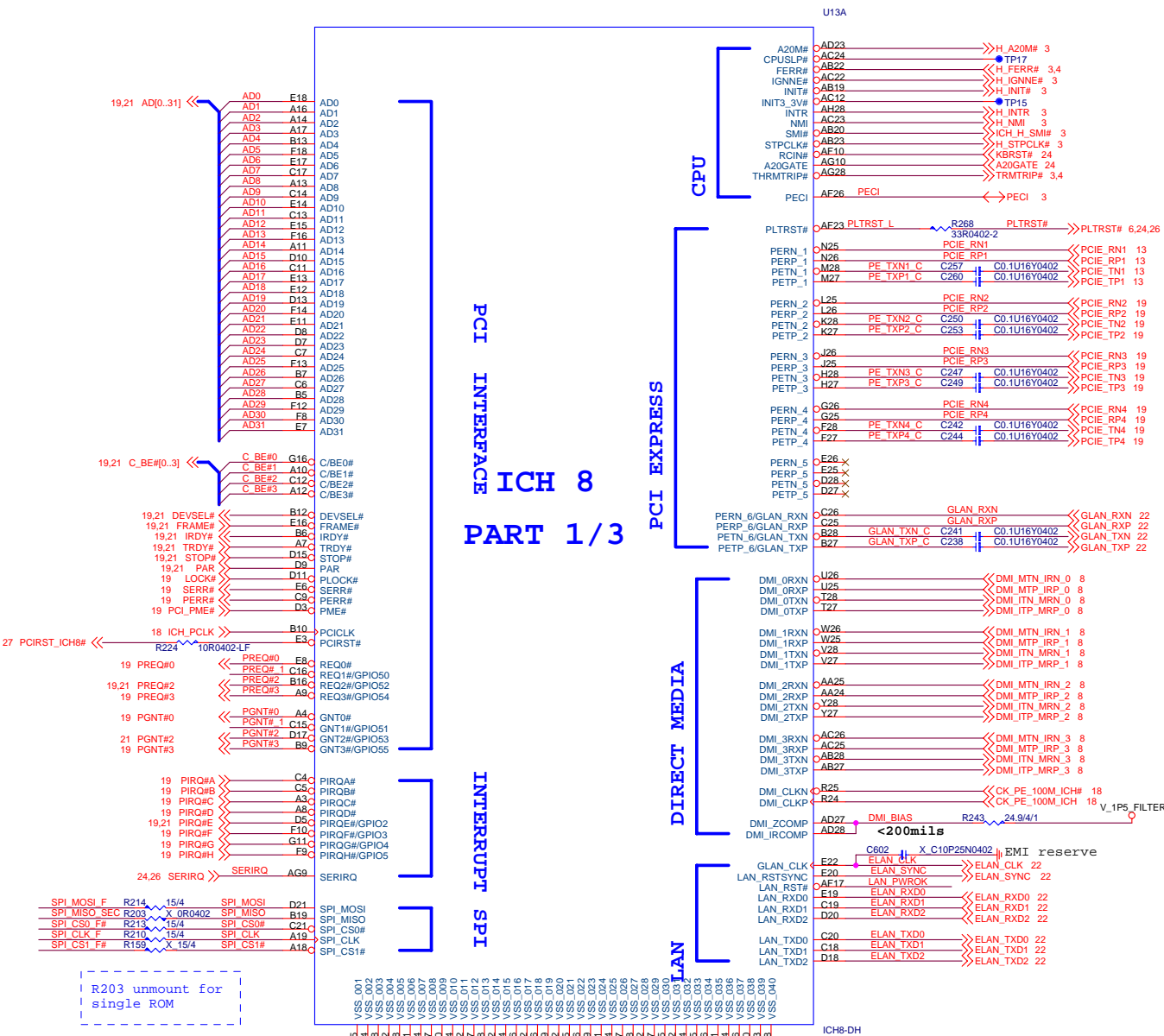
For EMI reserve



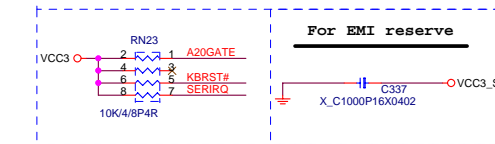
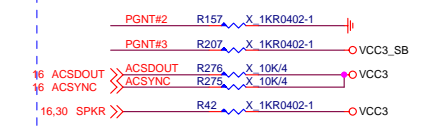
Video Connector



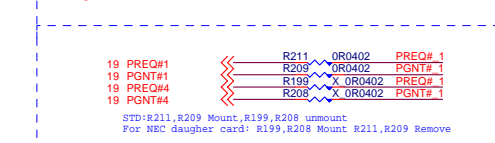
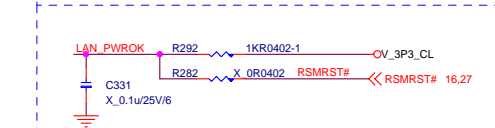
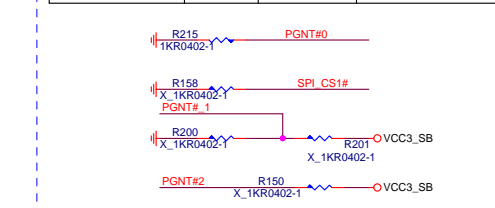
 MICRO-START INT'L CO.,LTD.		
Title VGA CONNECTOR		
Size	Document Number MS-7245	Rev 0B
Date: Monday, January 09, 2006	Sheet 14	of 35



ICH8 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRMEN	EN	DIS	INT VRM
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/PCIE	N/A	XOR MODE/PCIE PORT CONFIG
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG BIT 0 (5-6)

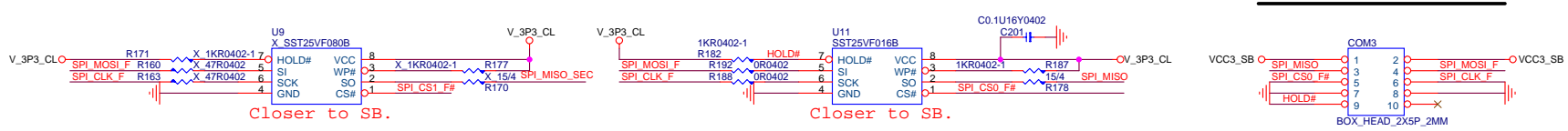


BOOT SELECT STRAPS			
BOOT DEVICE	GNT0	SPI_CS1#	JBOOT1
FWH	1	1	1-2
SPI	0	X	2-3(Default)
PCI	1	0	1-2 & R158



SPI FLASH(8M) (16M)

SPI Debug Port

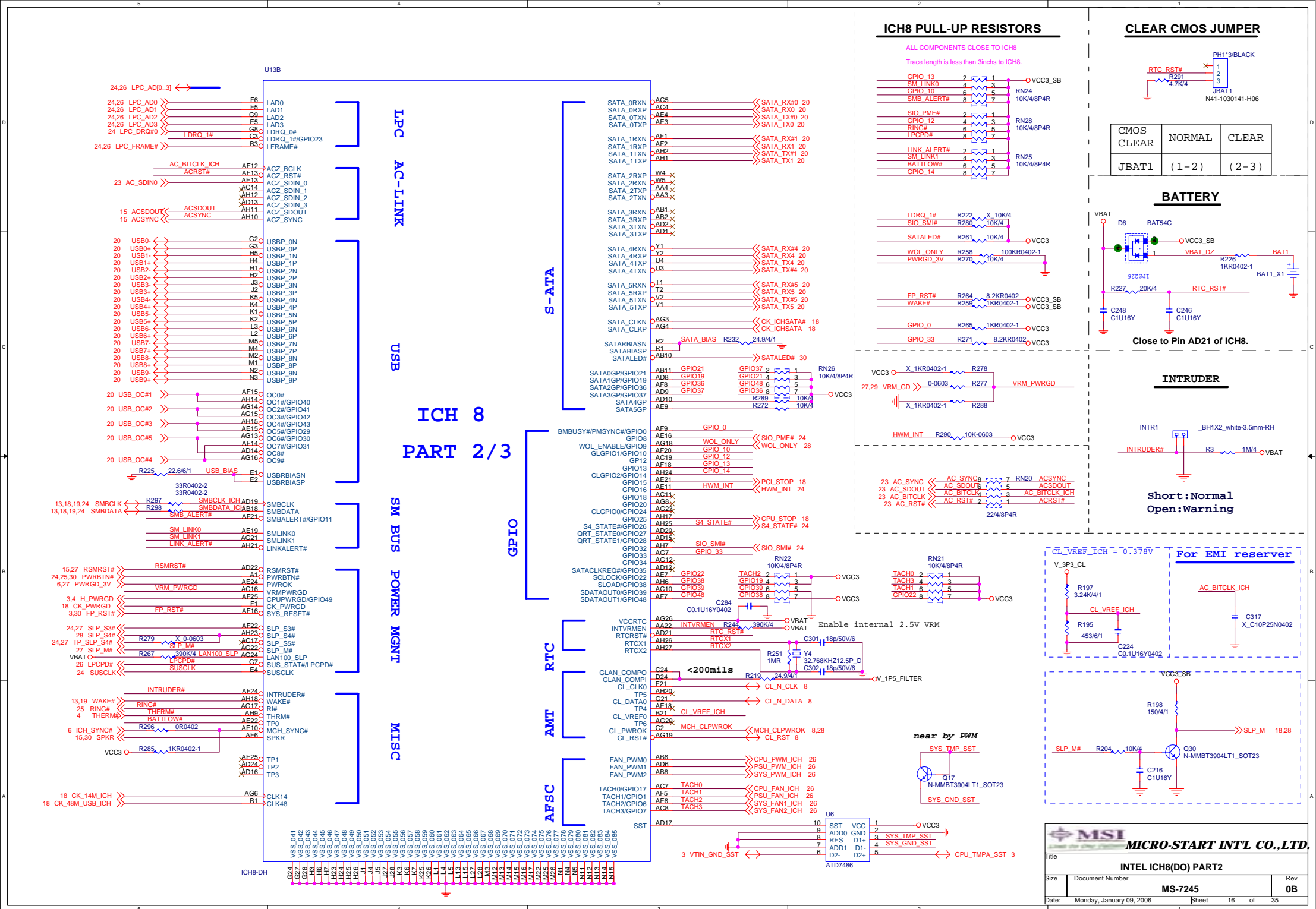


MICRO-START INTL CO.,LTD.

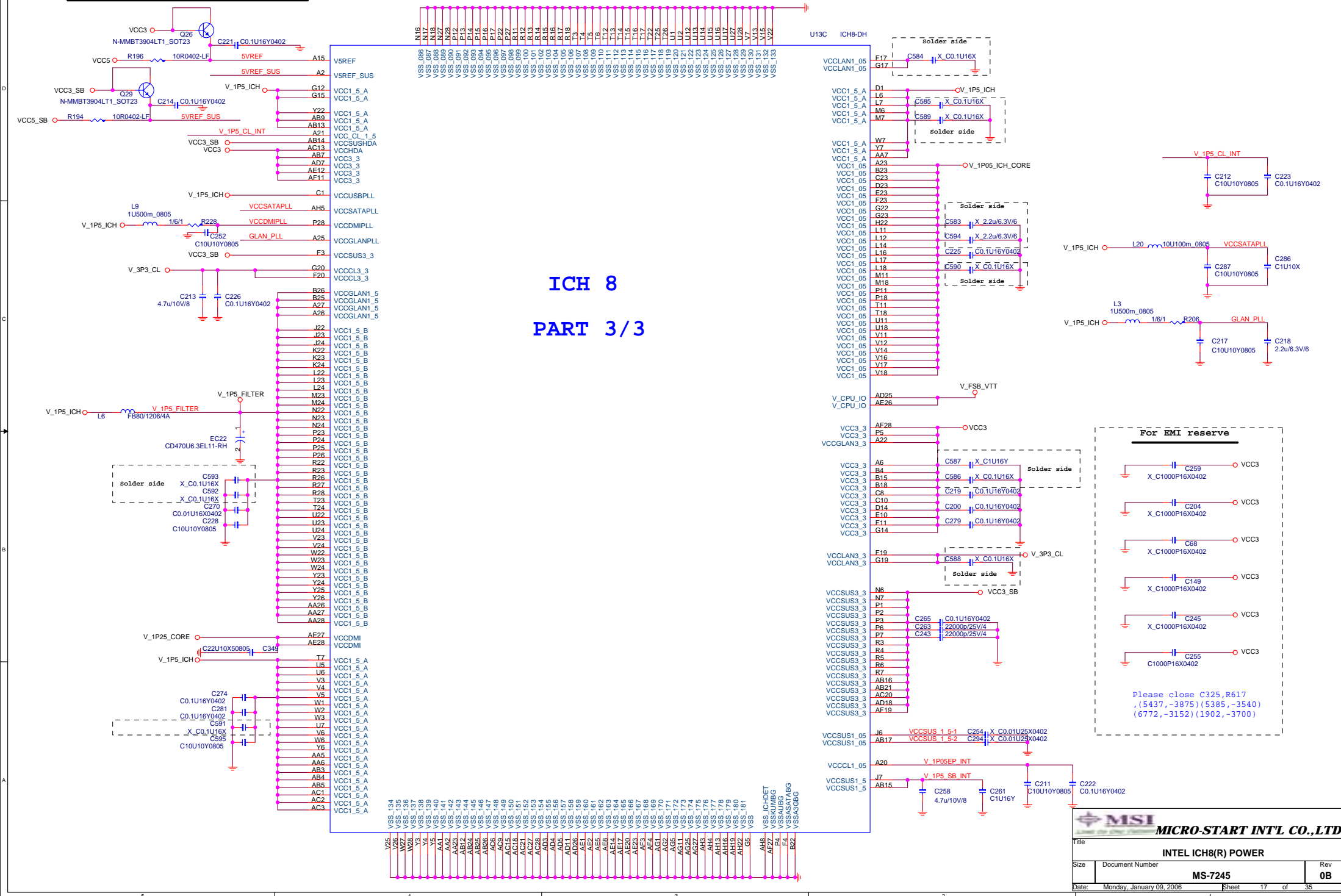
INTEL ICH8(R) PART1

Title: **MS-7245**
 Document Number: **MS-7245**
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Rev: **0B**



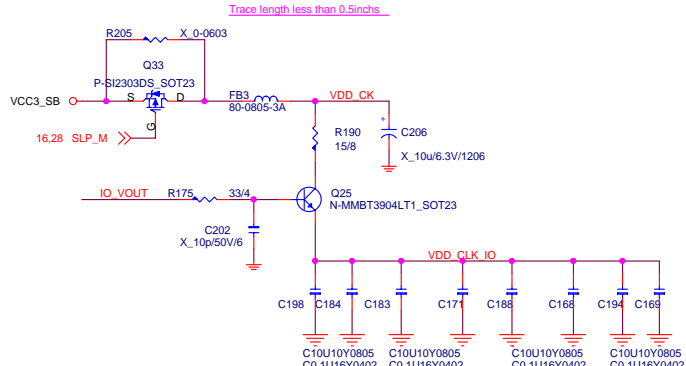
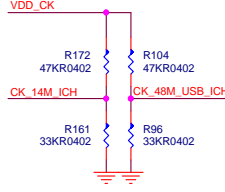
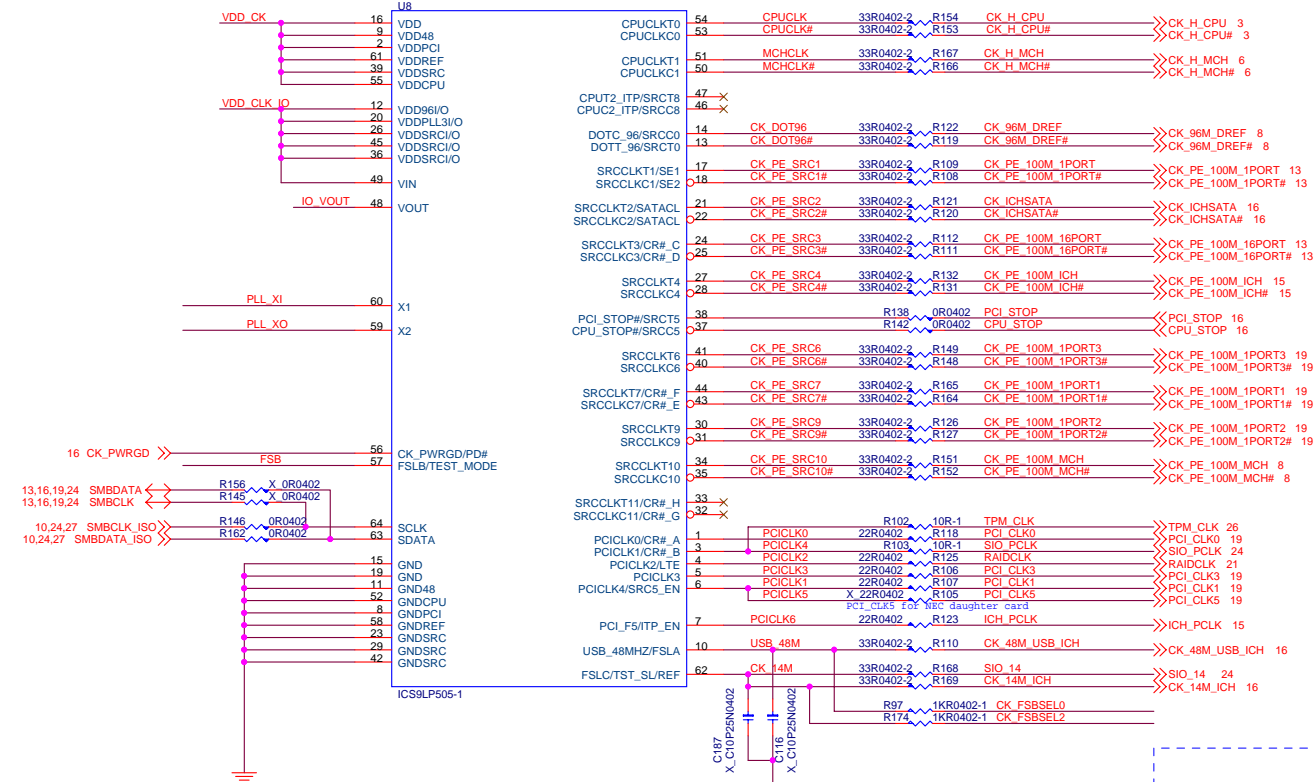
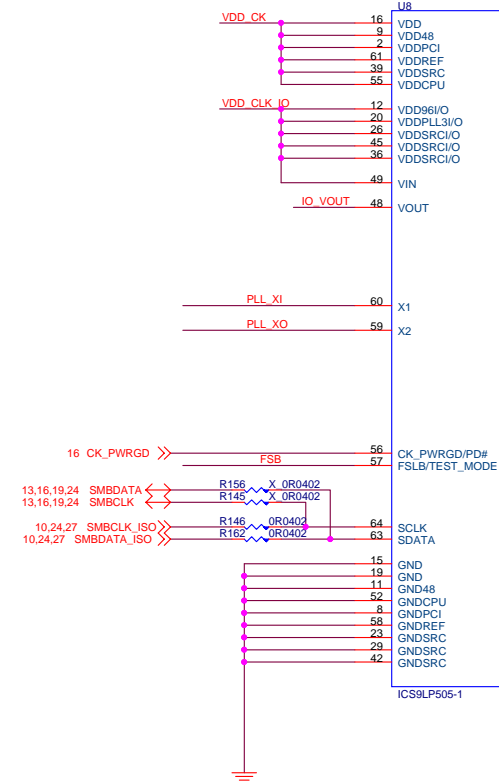
5VREF & 5VREF_SUS Sequencing Circuit



```

Please put all caps close CLK GEN.

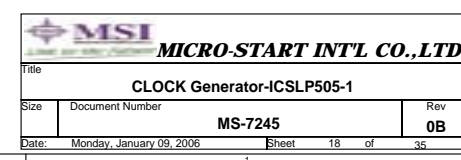
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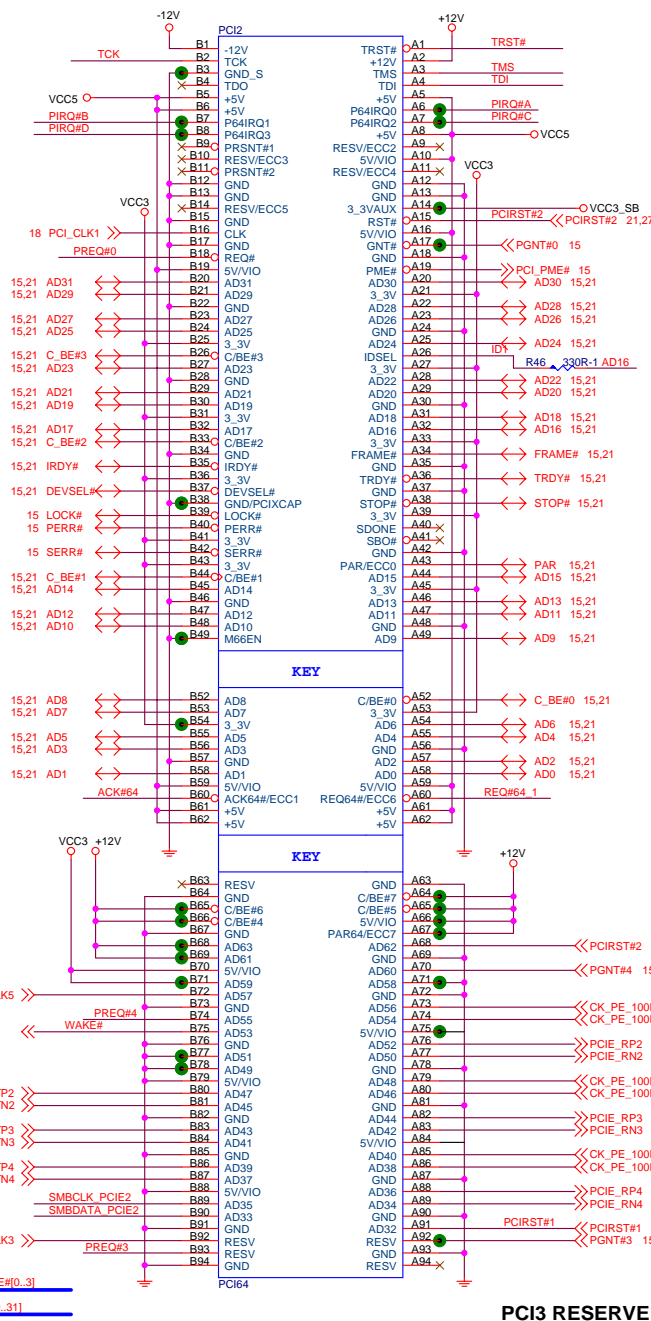


```

SRC5/SRC5# enable:stuff R113
output 100MHZ
CPU_STOP#,PCI_STOP#:stuff R124
input hi,low leave for iAMT
function.

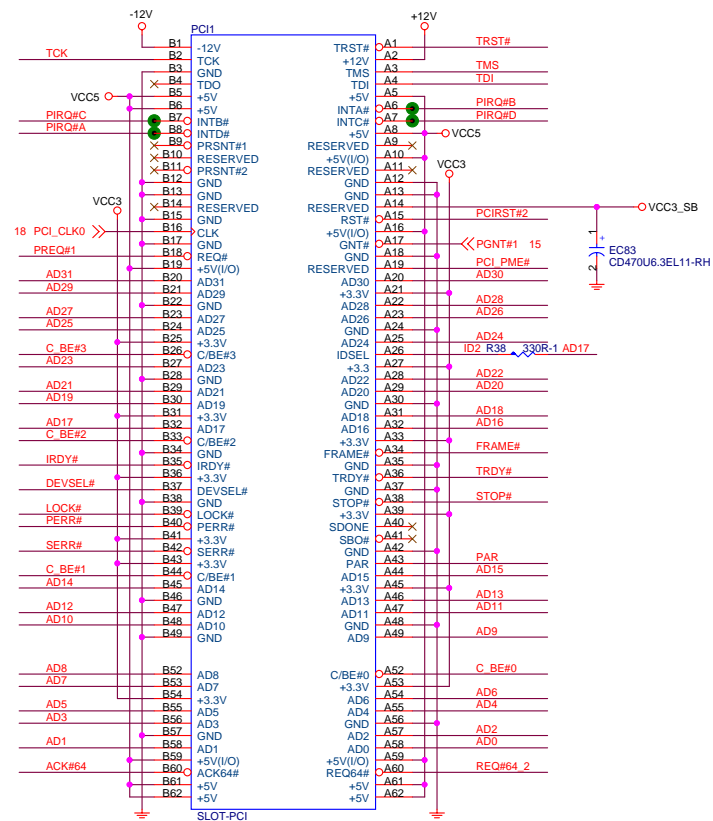
```



PCI1/PCIEXTENT

```
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A
```

```
PCI3 RESERVE
IDSEL = AD18
MASTER = PREQ#3
PIRQ#C
```

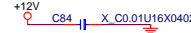
PCI SLOT 2 (PCI VER: 2.3 COMPLY)

```

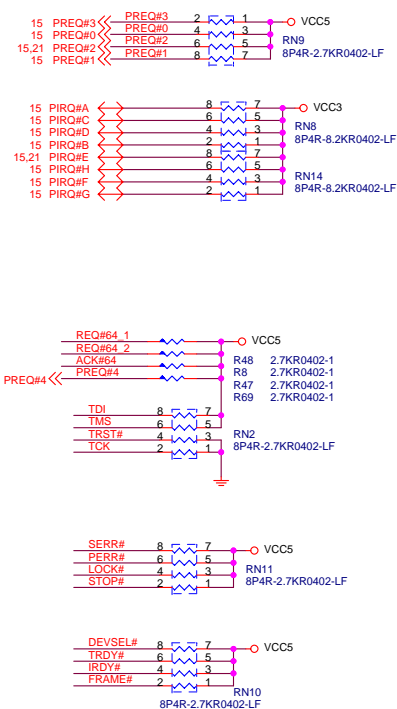
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

```

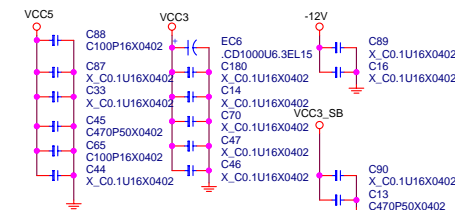
For EMI reserve



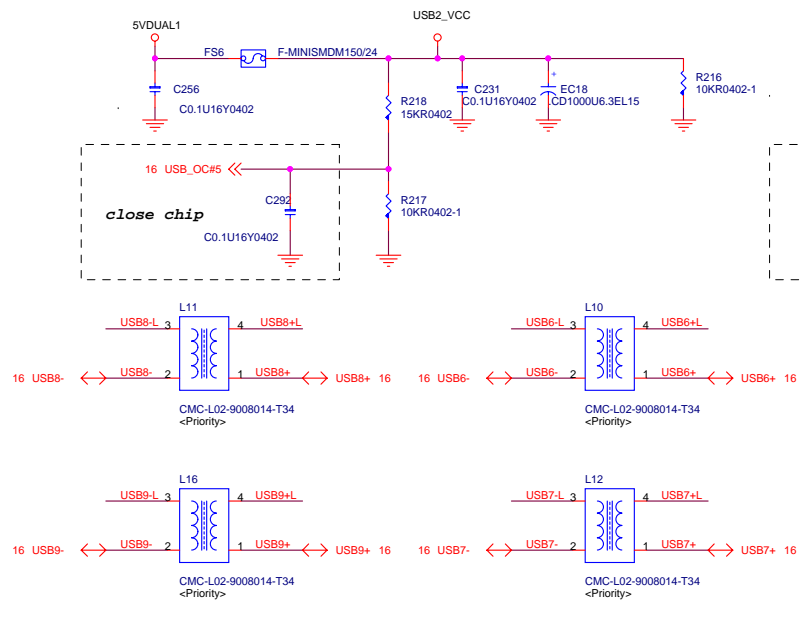
PCI PULL-UP / DOWN RESISTORS



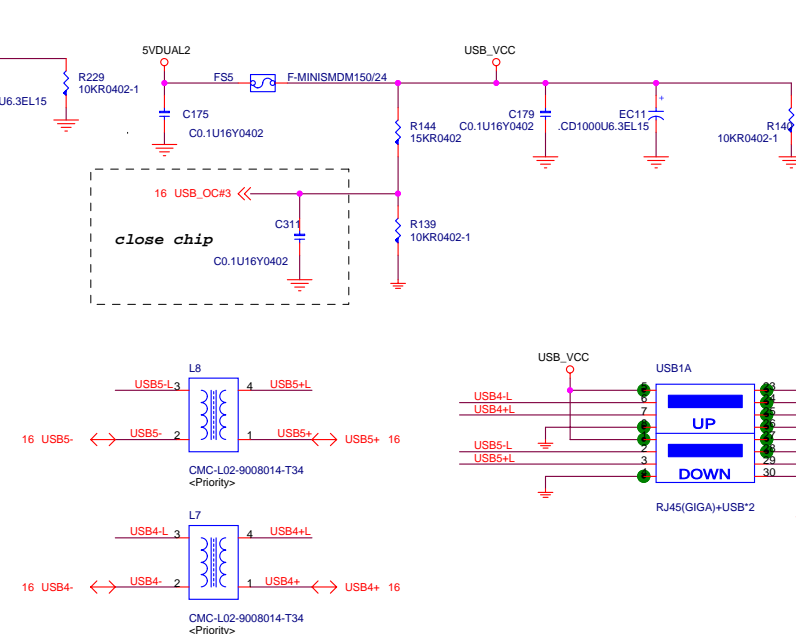
PCI SLOT DECOUPLING CAPACITORS



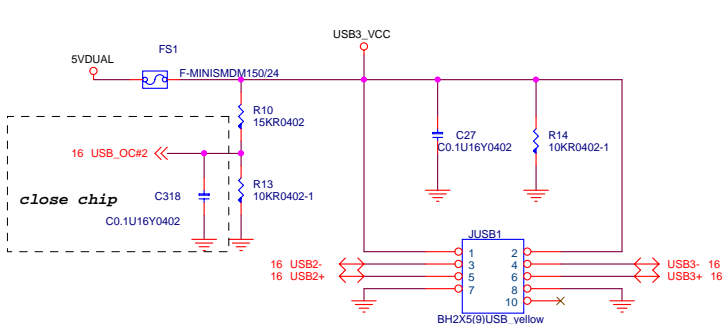
POWER CIRCUIT FOR USB PORT 6,7,8,9 (REAR)



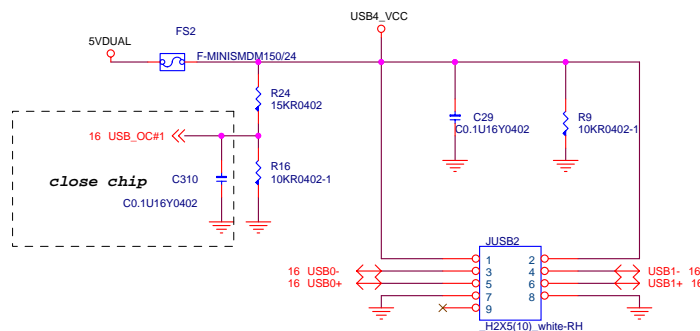
EXTERNAL USB PORT 4,5(REAR)



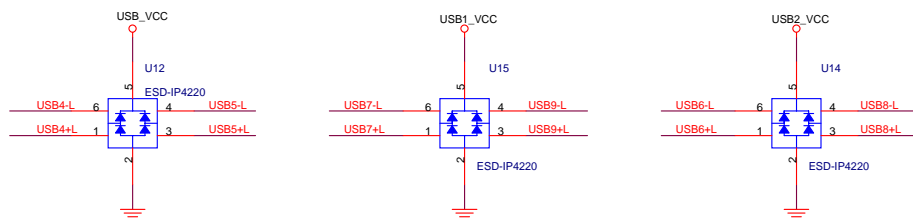
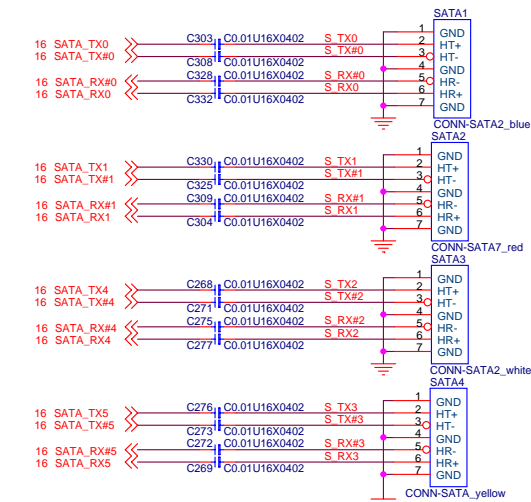
EXTERNAL USB PORT 2,3



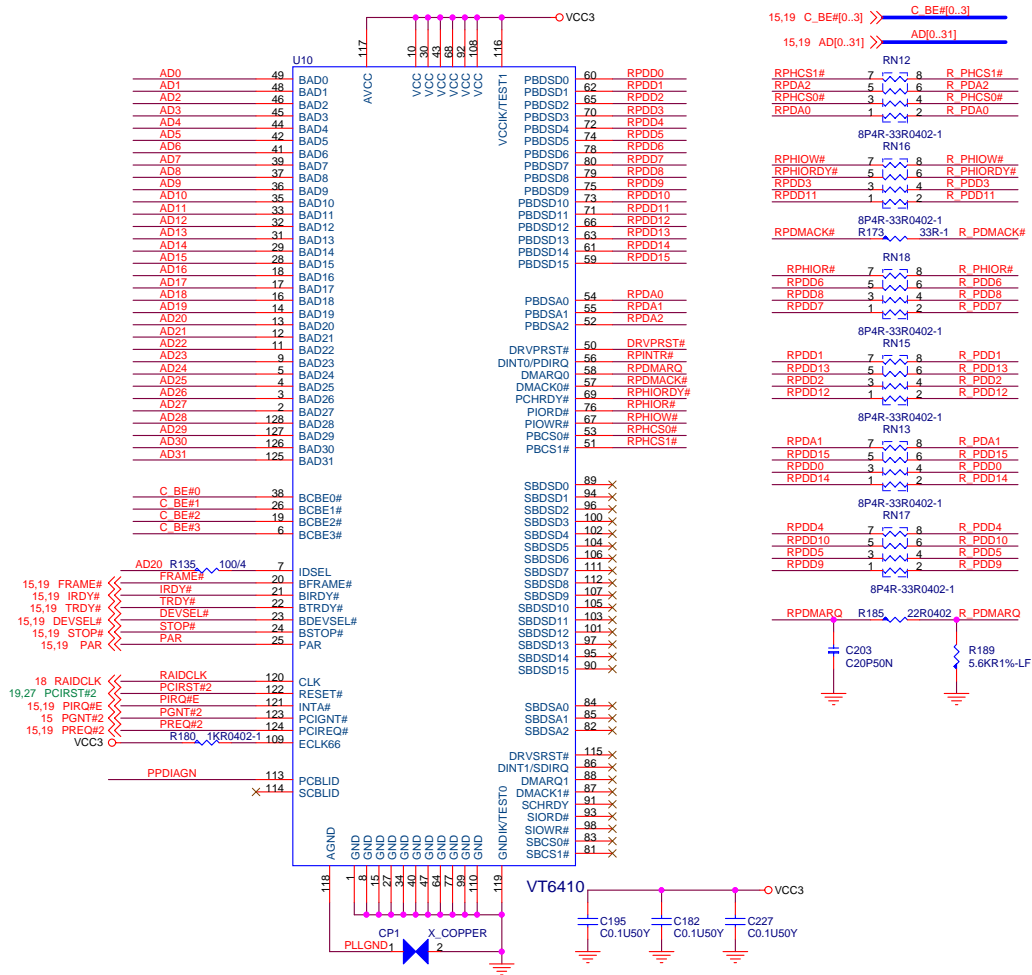
EXTERNAL USB PORT 0,1



SERIAL ATA CONNECTOR BLOCK

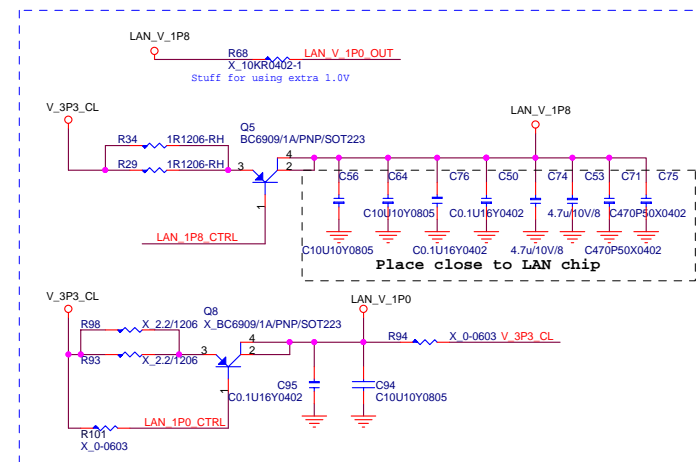
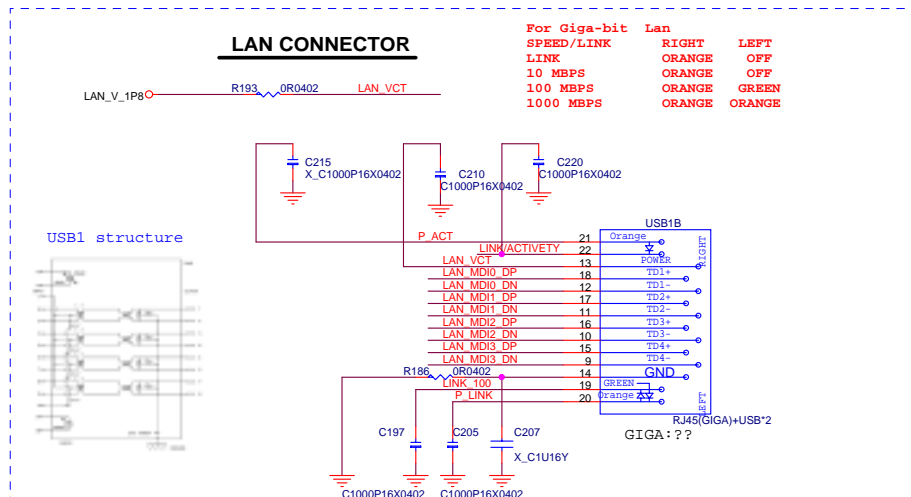
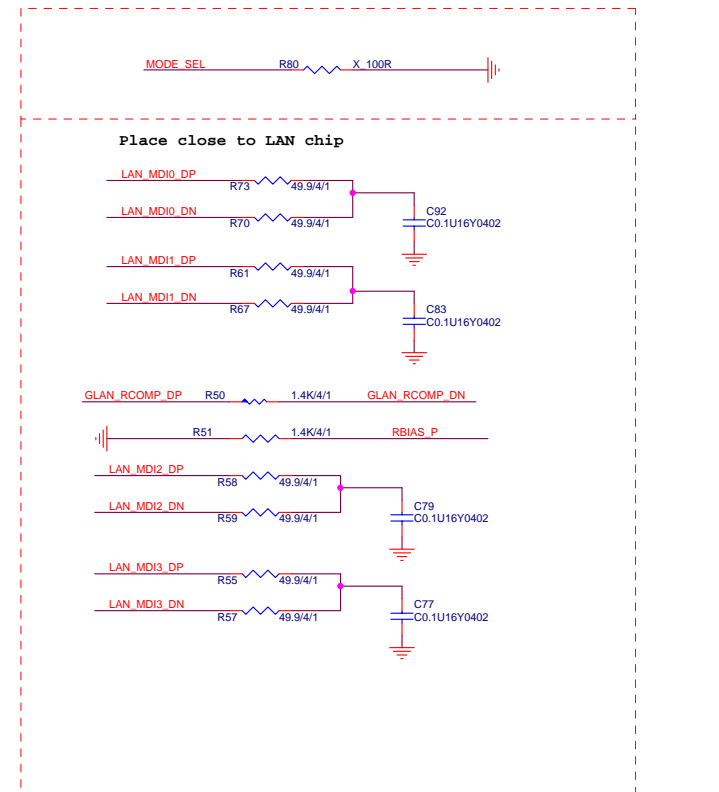
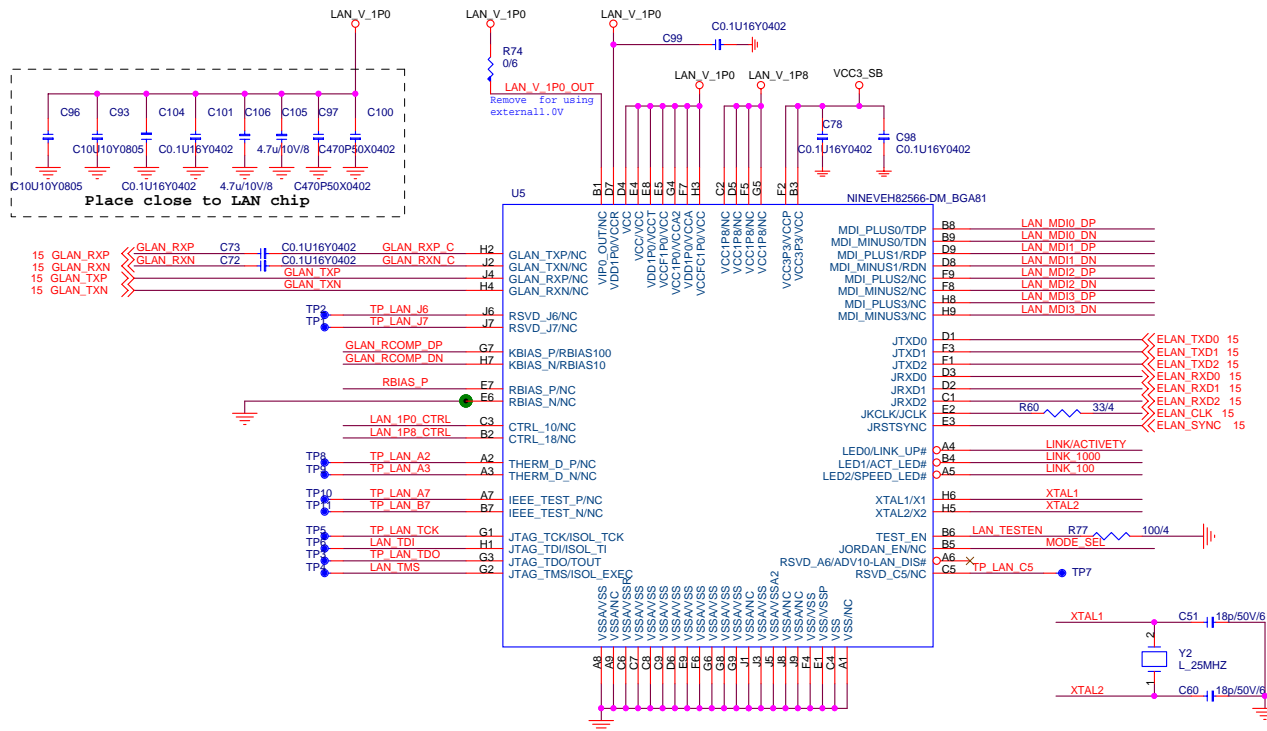


For EMI reserve
VCC5
C341 C1000P16X0402
please close SATA2 connector



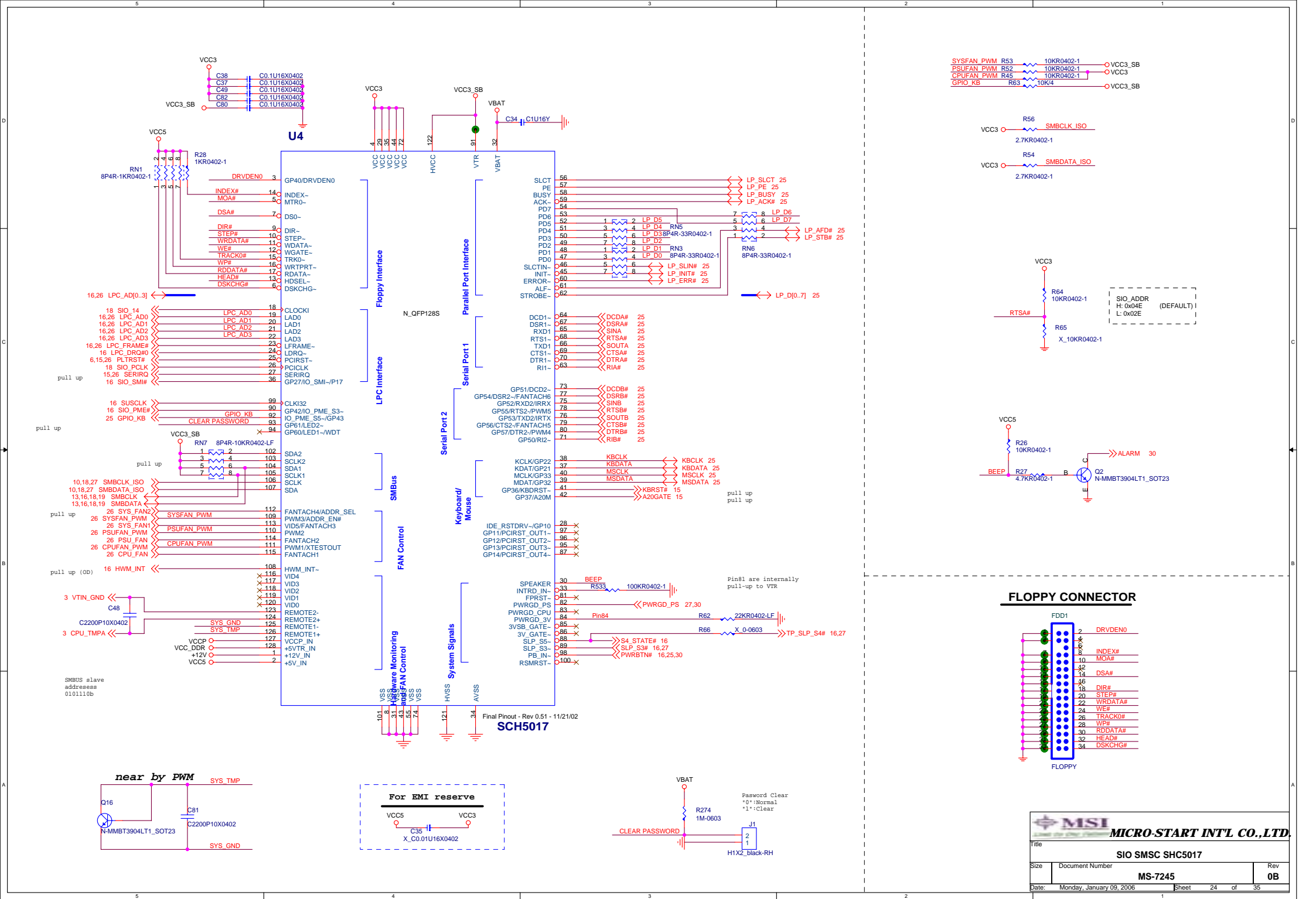
IDSEL = AD20
MASTER = PREQ#2
PIRQ#E

LAN - NINEVEH

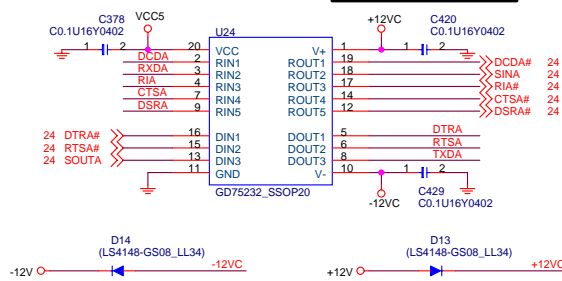


ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

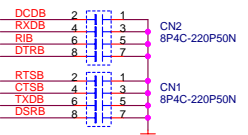
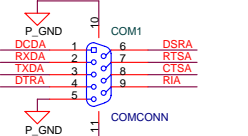
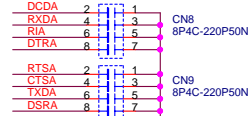
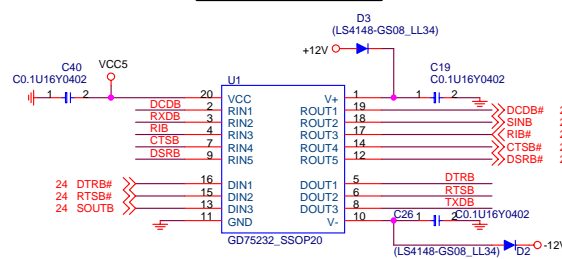




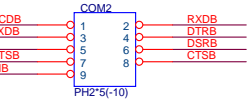
SERIAL PORT 1



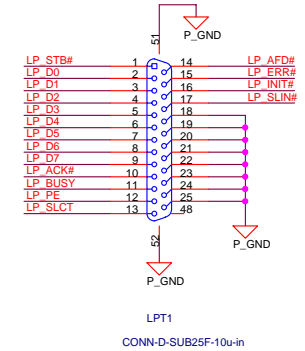
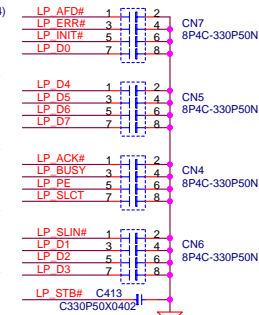
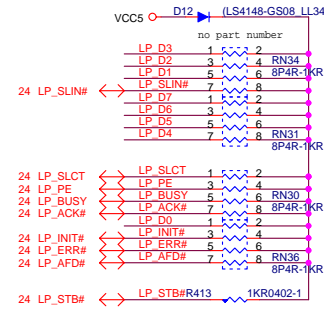
SERIAL PORT 2



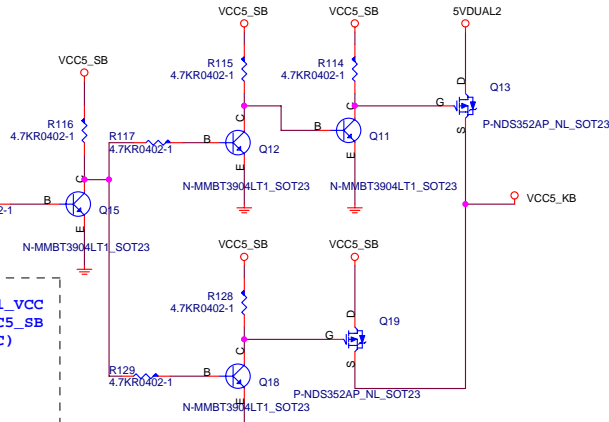
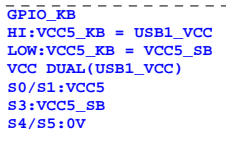
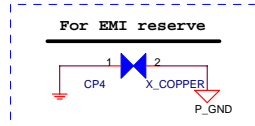
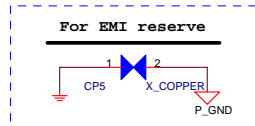
COM2 HEADER



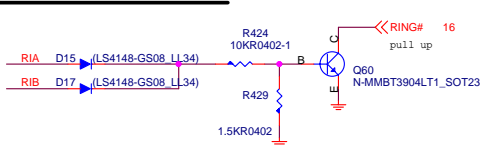
PARALLAL PORT



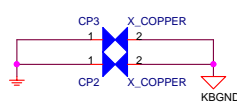
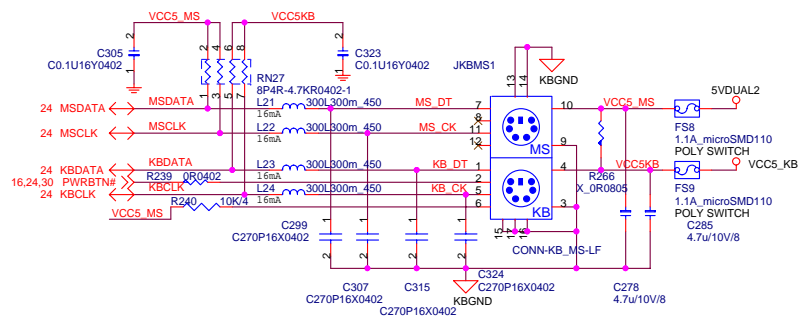
K/B Power supply function for NEC



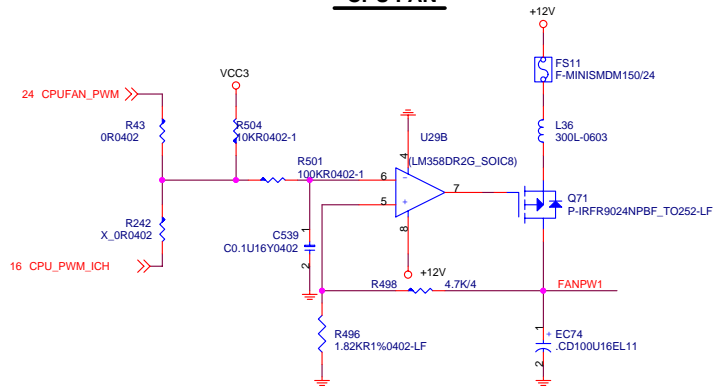
Wake On Modem Header



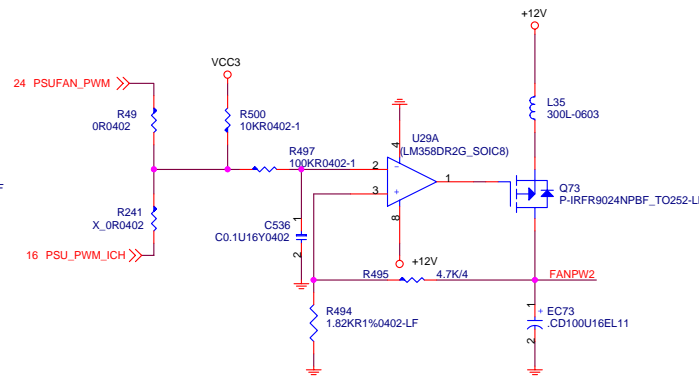
PS2 KEYBOARD & MOUSE CONNECTOR



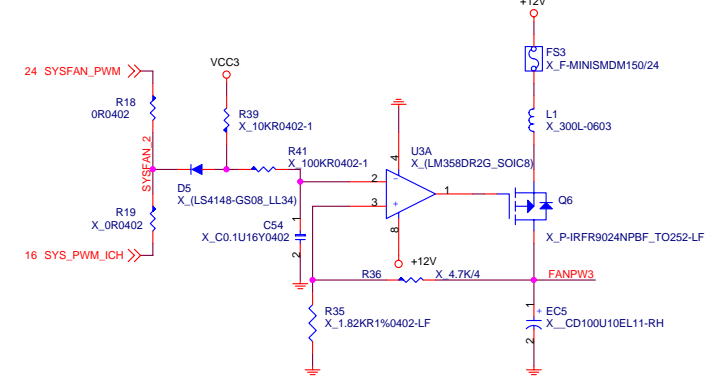
CPU FAN



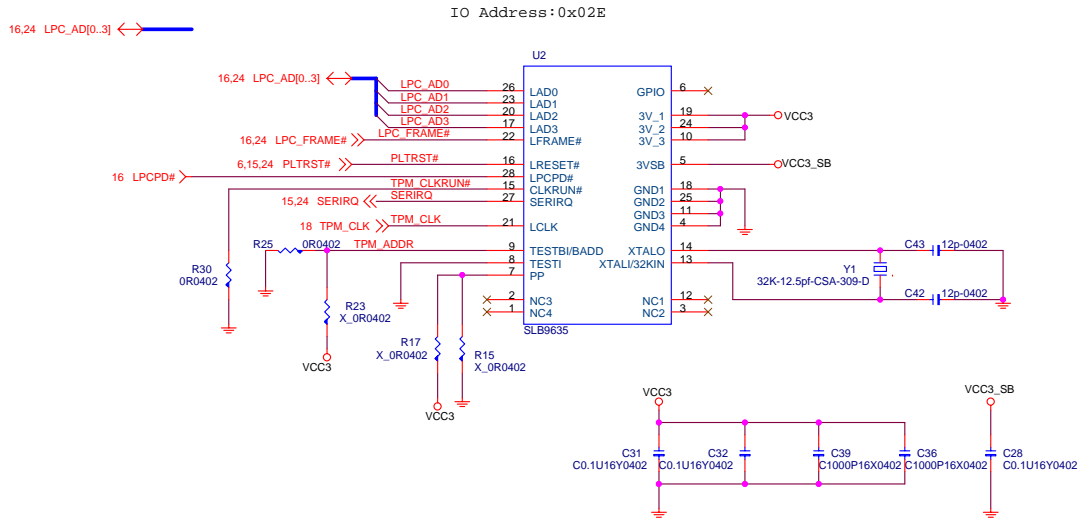
PSU FAN



SYS FAN1



TPM 1.2



For EMI reserve

VCC5
C346 C0.1U16Y0402

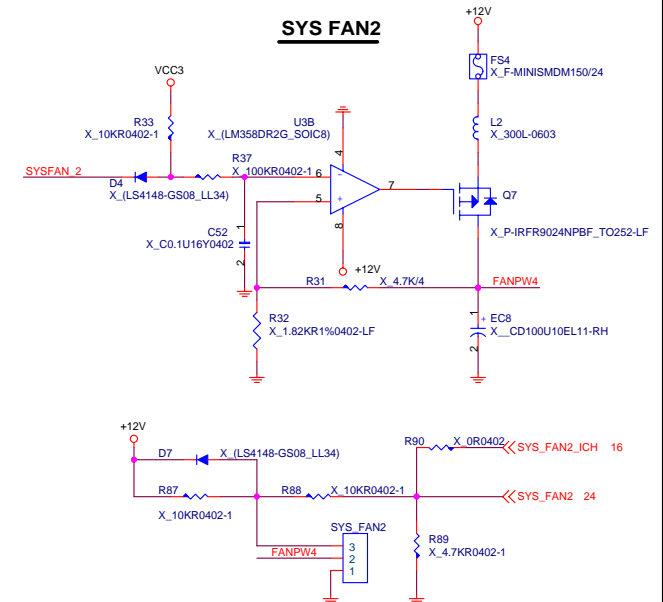
Please close (-1905 -1465)

For EMI reserve

VCC5
C85 X_C0.1U16Y0402

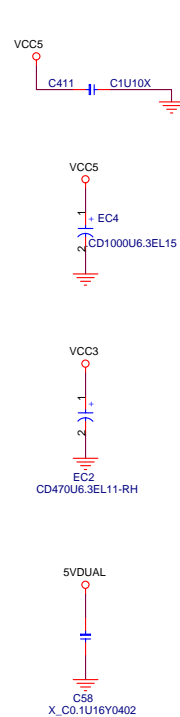
Please close (-2450 5020)

SYS FAN2

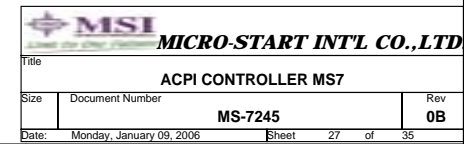


3VSB MODE SELECT	
3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

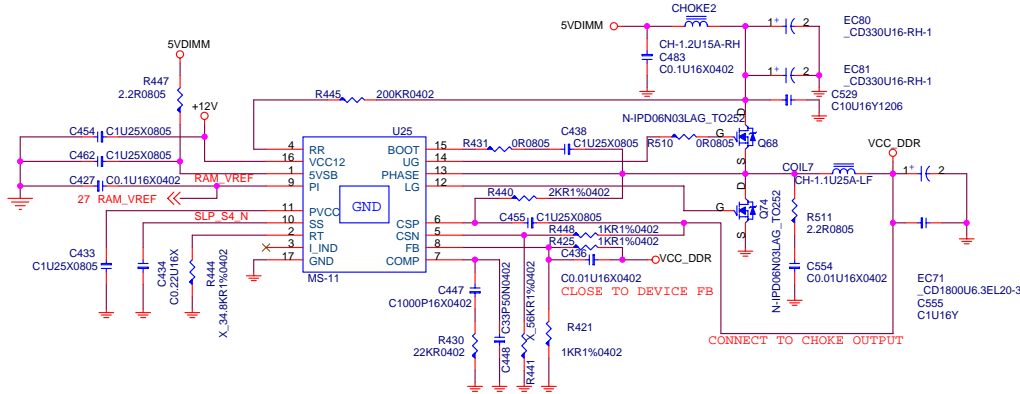
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH



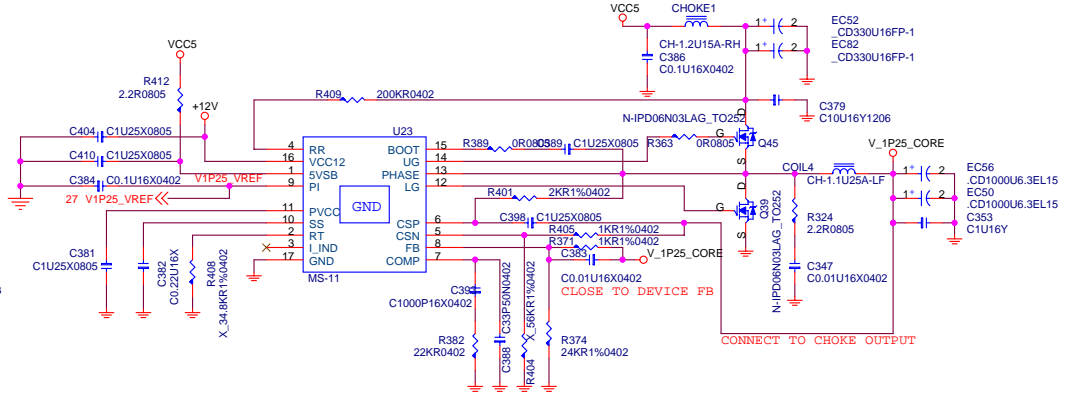
The schematic diagram shows the U30 W83310DG SOP8-LF chip. The chip is a blue square with pins 1-8 on the top and bottom. Pin 1 is VREF2, Pin 2 is VIN, Pin 3 is VCTRL, Pin 4 is VREF1, Pin 5 is BOOT_SEL, Pin 6 is GND2, Pin 7 is ENABLE, Pin 8 is VREF2. The chip is connected to VCC3_SB, VCC_DDR, VTT_DDR, and GND. Various capacitors (C541, C559, EC69, EC70) and resistors (R516, R517) are shown.

[illegible][illegible]

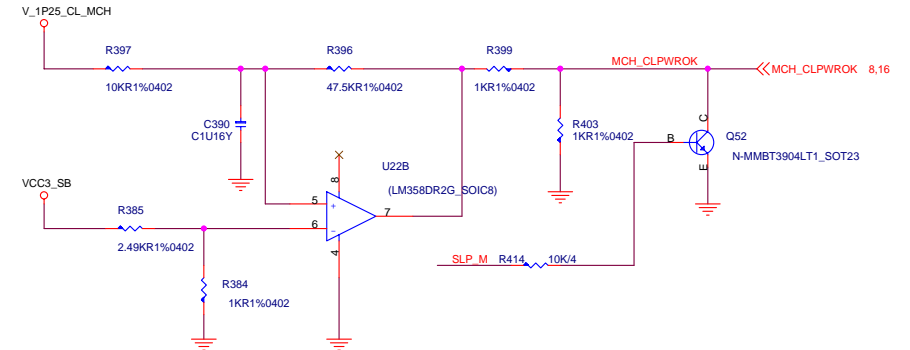
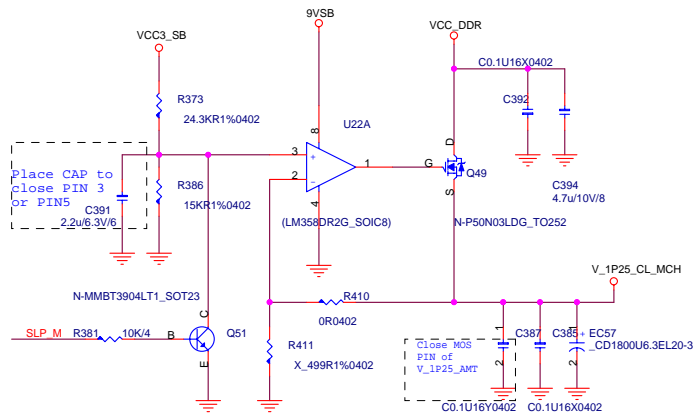
1.8V POWER (25A)



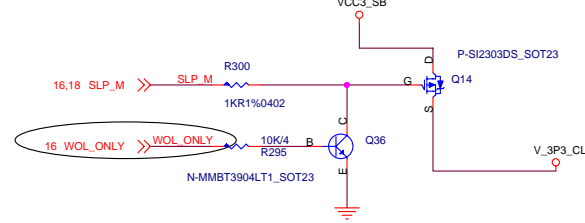
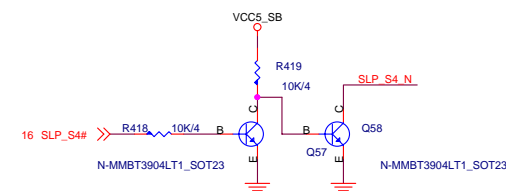
GMCH/ICH8 1.25V POWER (21.3A)



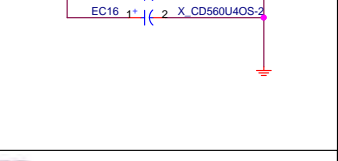
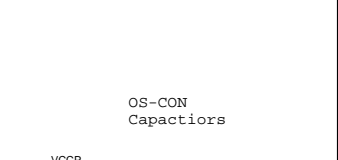
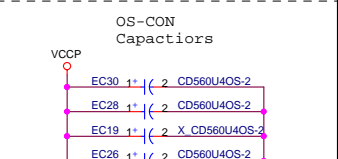
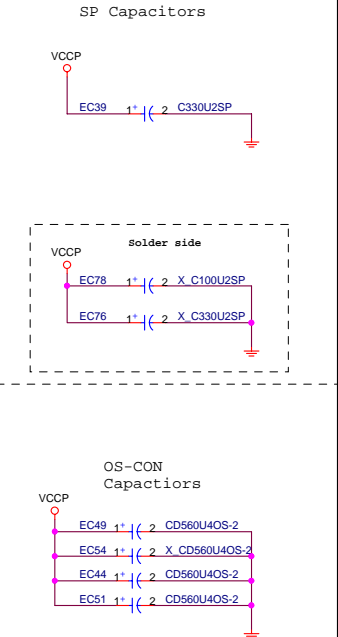
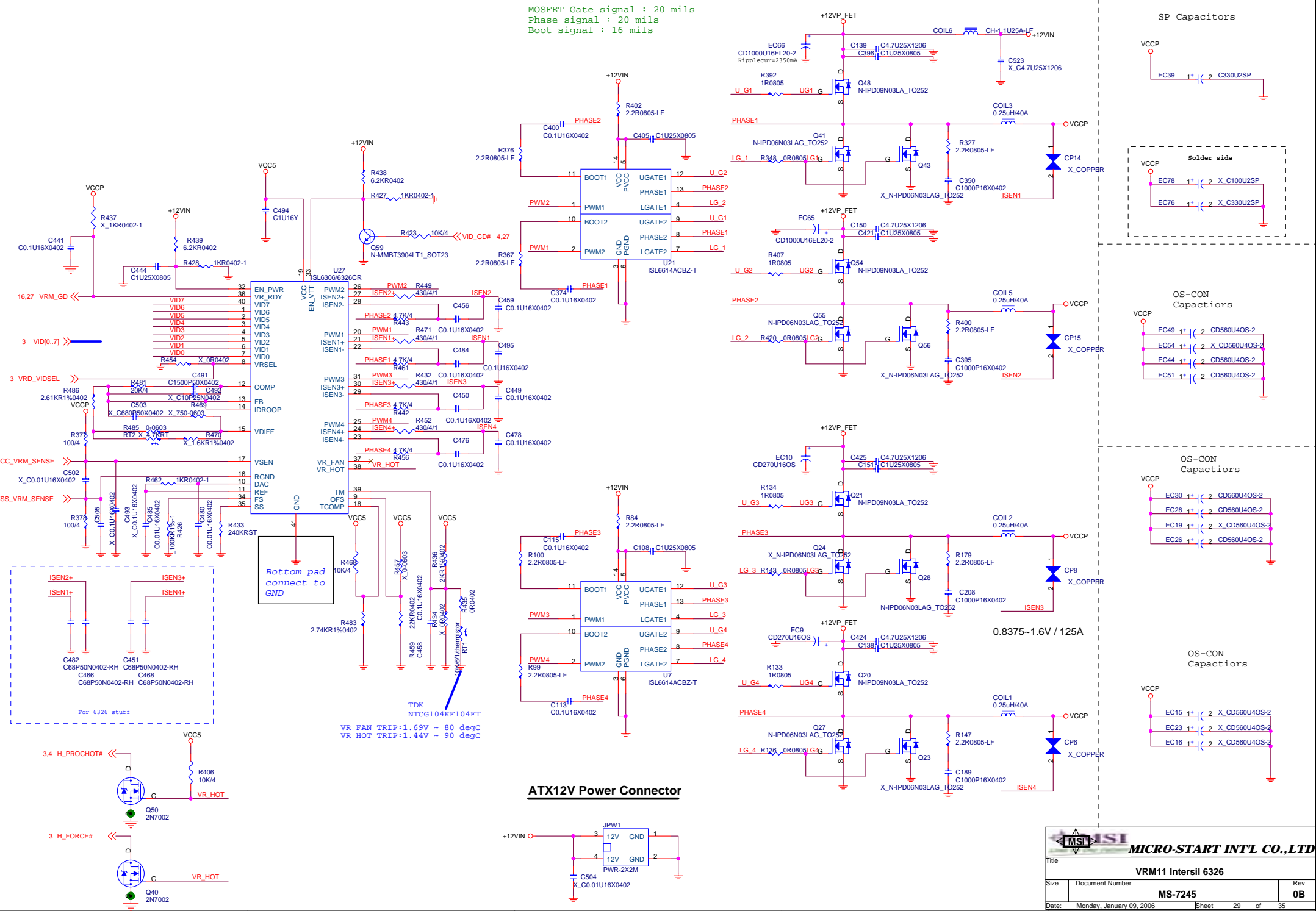
V_1P25_CL_MCH (3.8A)



SLP_S4#
 AMT Disable-->indicate ACPI S4 state, DRAM power off.
 AMT Enable-->not be asserted ACPI S4 state, DRAM power ON
 AMT Enable SLP_MH-->Control the overall power to Intel
 AMT during ACPI S3-S5.
 S4_SATE#
 AMT Enable-->indication of ACPI S4 state

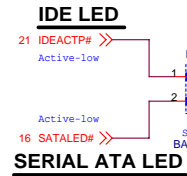


MOSFET Gate signal : 20 mils
Phase signal : 20 mils
Boot signal : 16 mils

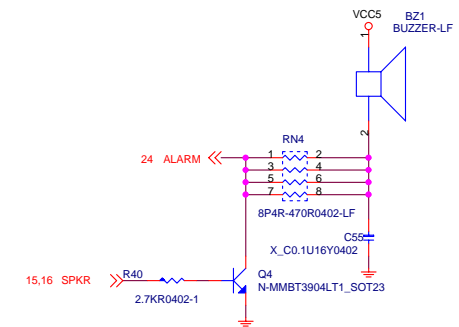


MICRO-START INTL CO.,LTD.		
Title		
VRM11 Intersil 6326		
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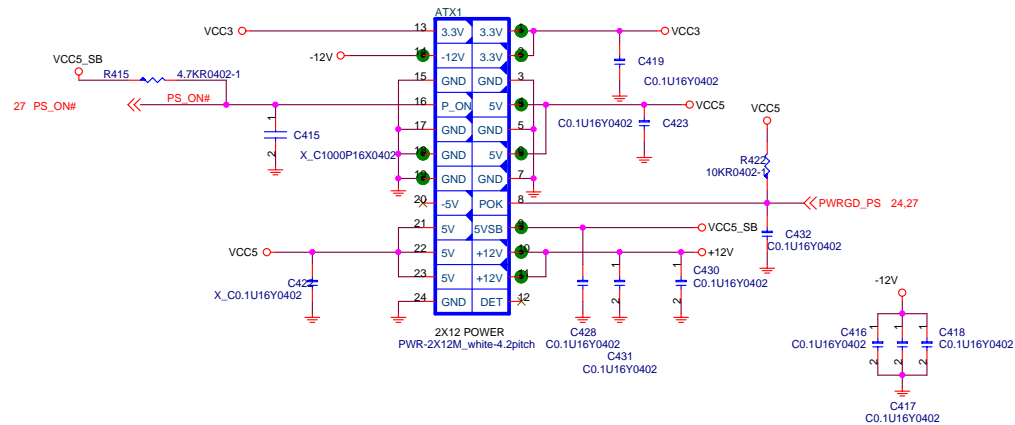
Front Panel



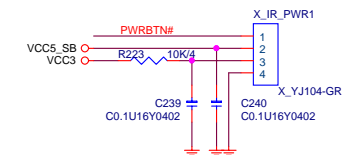
SPEAKER



ATX Connector



For NEC IR POWER



ICH8

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF9
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF5
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 10K	VCC3		D5
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 10K	VCC3		F10
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 10K	VCC3		G11
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 10K	VCC3		F9
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE6
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AC8
GPIO 8	I/O	GPI	SIO_PME# connect to SIO,pull_up VCC3_SB with 10k	VCC3_SB	UNMUXED	AE16
GPIO 9	I/O	MGPIO3	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AG18
GPIO 10	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AF20
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		AF21
GPIO 12	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VBT	UNMUXED	AC19
GPIO 13	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	UNMUXED	AF18
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AH24
GPIO 15	I/O	GPO	PCI_STOP	VCC3_SB	UNMUXED	AE21
GPIO 16	I/O	GPO	SIO HWM_INT,pull_up VCC3 with 10K(change to GPI)		UNMUXED	AE11
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AC7
GPIO 18	I/O	GPO	NC		UNMUXED	AC11
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AD8
GPIO 20	I/O	GPO	NC		UNMUXED	AG8
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AB11
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE7
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull_up VCC3 with 10K	VCC3	MUXED	C3
GPIO 24	I/O	GPO	NC		MUXED	AG23
GPIO 25	I/O	GPO	CPU_STOP	3.3V_SB	UNMUXED	AH17
GPIO 26	I/O	GPO	S4 STATE			AH25
GPIO 27	I/O	GPO	NC	3.3V_SB		AD20
GPIO 28	I/O	GPO	NC			AD15
GPIO 29	I/O	OC5#	OC#3 connect to USB connector	3.3V_SB		AE15
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		AG13
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		AF14
GPIO 32	I/O	GPO	SIO_SMI# connect to SIO,pull up VCC3 with 10k	VCC3	UNMUXED	AH7
GPIO 33	I/O	GPO	Pull-up to VCC3 with 8.2K		UNMUXED	AG7
GPIO 34	I/O	GPO	NC		UNMUXED	AG12
GPIO 35	I/O	GPO	NC			AD12
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF8
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD9
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH6
GPIO 39	I/O	GPI	Pull-down to GND with 10K directly	VCC3		AC10
GPIO 40	I/O	OC1#	OC#1 connect to USB connector	VCC3		AH14
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	VCC3		AG14
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	VCC3		AG15
GPIO 43	I/O	OC4#	OC#3 connect to USB connector	VCC3		AH15
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF7
GPIO 49	I/O	CPU_PWRGD	H_PWRGD connect to CPU	VTT_OUT		AF25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 10K	VCC5	MUXED	C16
GPIO 51	I/O	GNT1#	GNT1#		MUXED	A15
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 10K	VCC5	MUXED	B16
GPIO 53	I/O	GNT2#	GNT2#		MUXED	D17
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 10K	VCC5	MUXED	A9
GPIO 55	I/O	GNT3#	GNT3#		MUXED	B9

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI1 EXTENT	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK1
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK0
VT6410	PIRQ#E	PREQ#2 PGNT#2	AD20	RAIDCLK
PCI3	RESERVED	PREQ#3 PGNT#3	AD18	PCI_CLK3

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A1/SCLK_A1# SCLK_A2/SCLK_A2#
DIMM 2	0A2H	SCLK_A3/SCLK_A3# SCLK_A4/SCLK_A4# SCLK_A5/SCLK_A5#
DIMM 3	0A4H	SCLK_B0/SCLK_B0# SCLK_B1/SCLK_B1# SCLK_B2/SCLK_B2#
DIMM 4	0A6H	SCLK_B3/SCLK_B3# SCLK_B4/SCLK_B4# SCLK_B5/SCLK_B5#

SIO SCH5017


PIN NAME	PIN#	USAGE	Input/Output
GP43	92	GPIO_KB	OUTPUT
GP27	36	SIO_SMI#	OUTPUT
GP42	90	SIO_PME#	OUTPUT
GP61	93	CLEAR_PASSWORD	INPUT

SMBus DISTRIBUTION

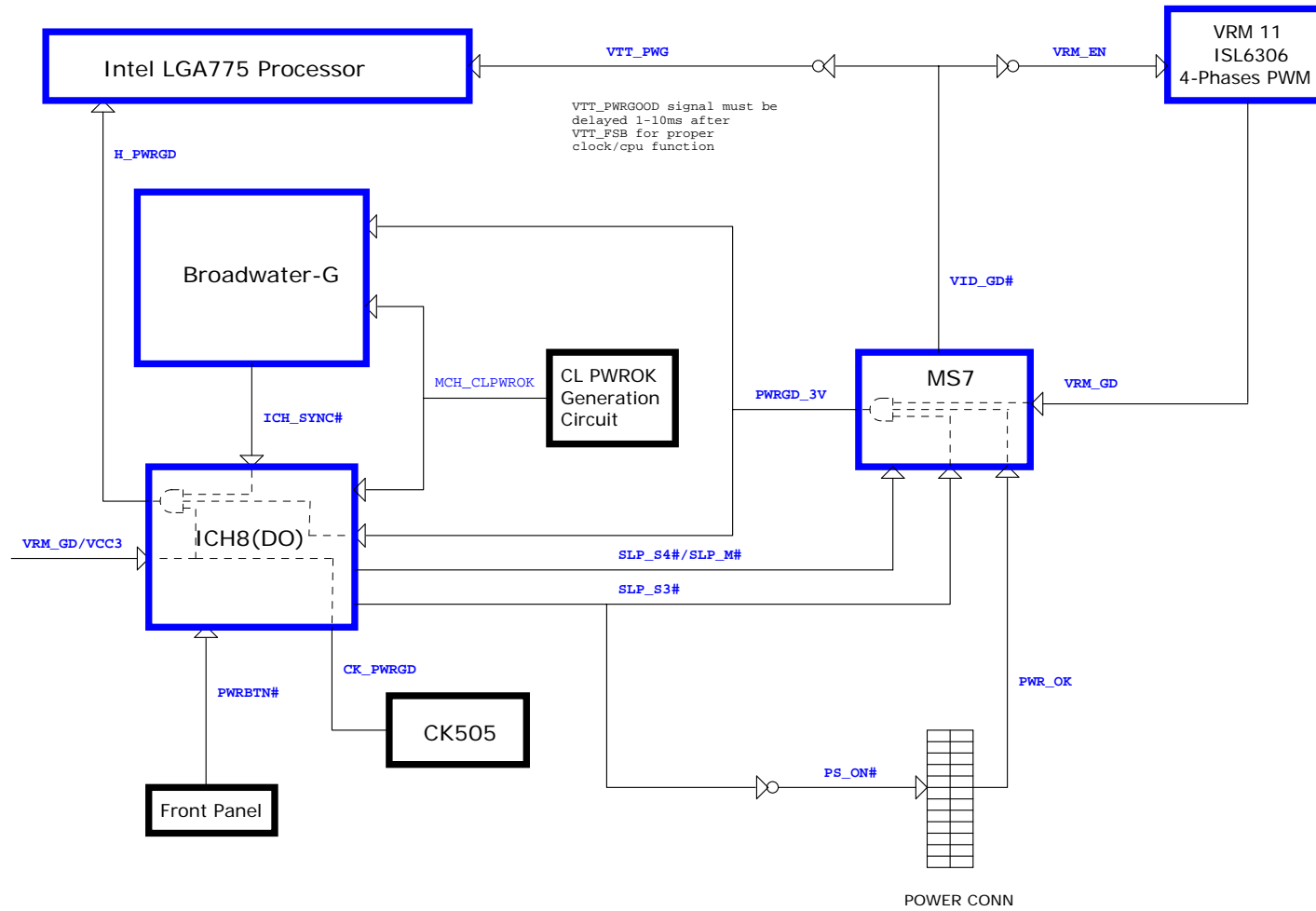
SMBus	Power	Load
SMBCLK	VCC3_SB	ICH8, SIO,PCI EXPRESS x16,x1
SMBCLK_ISO	VCC3	DIMM, CLK GEN, SIO, MS7,LAN

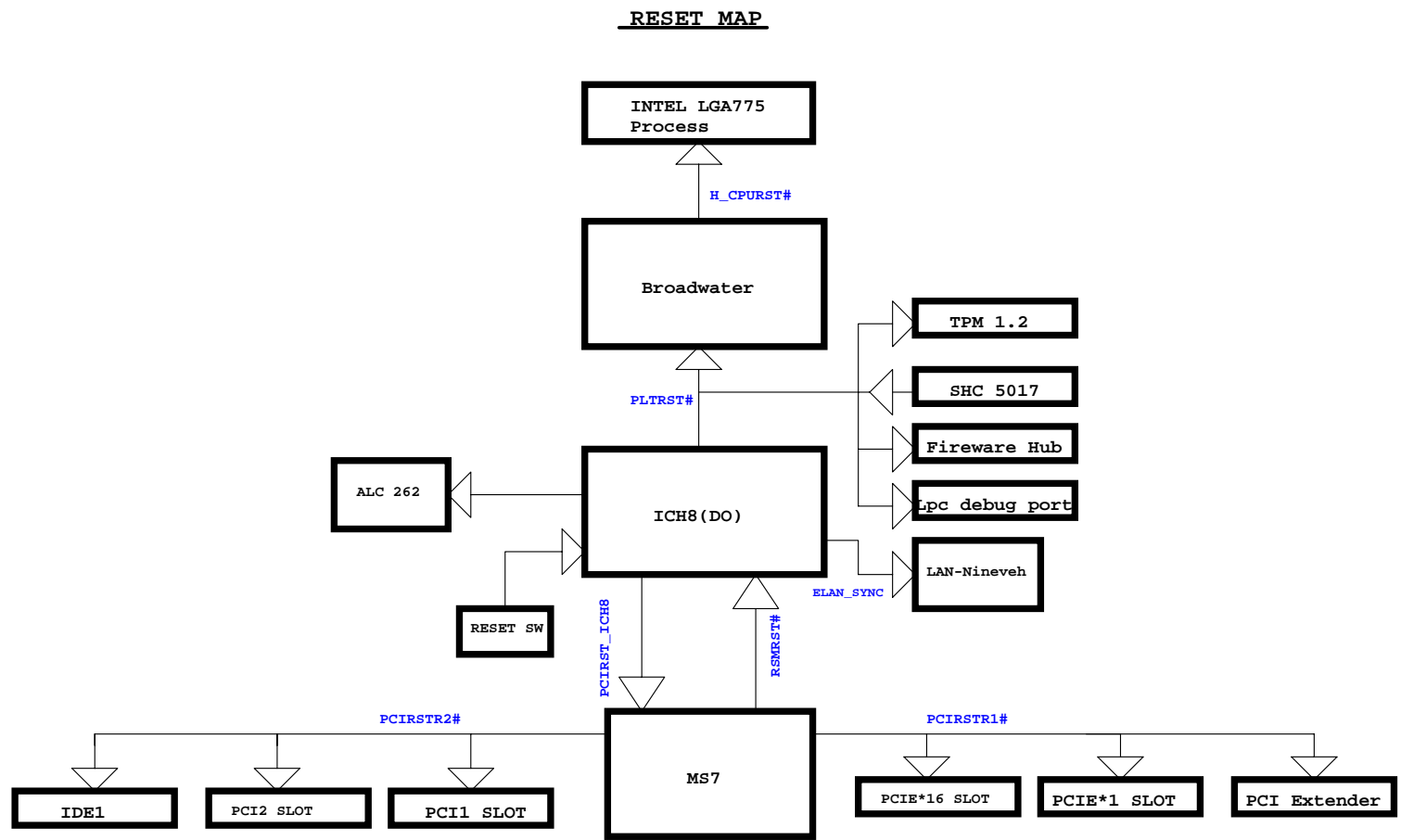
JUMPER SETTING

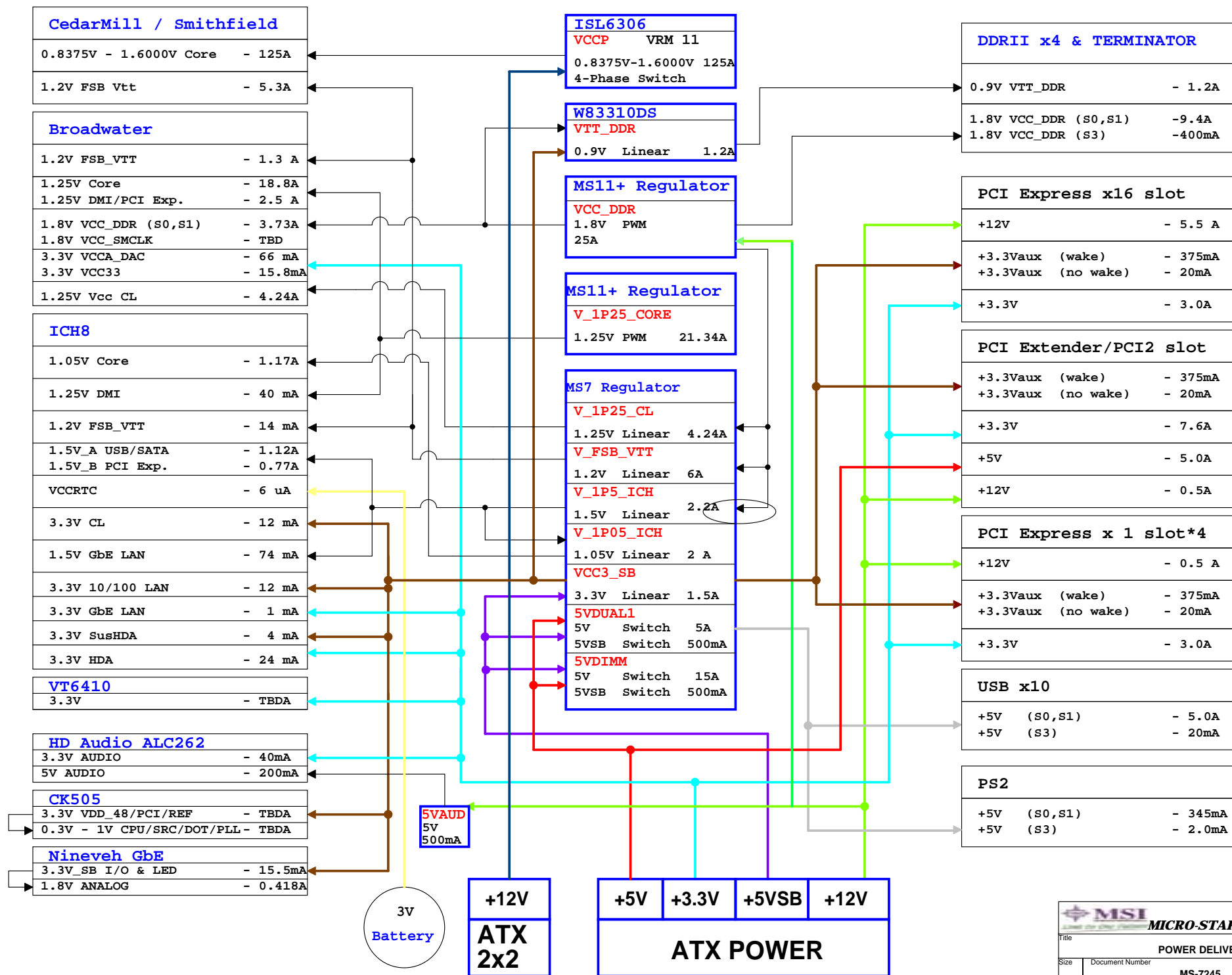
JBAT1	(1-2)Normal	(2-3)Clear
INTRUDER	Short Normal	Open warning
JPWD1	(1-2)Clear	Open Normal

 MICRO-START INTL CO.,LTD.		
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GPIO PIN definition		
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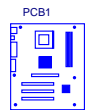
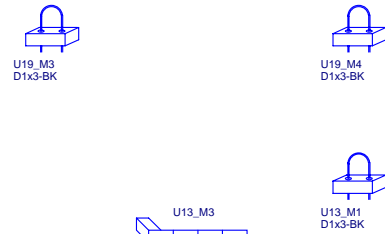
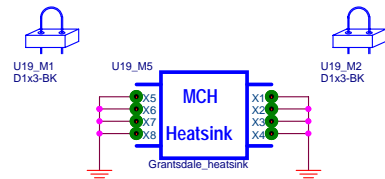
PWROK MAP







MANUAL PART



MS-7245-0B, GREEN



BATTERY HOLDER, 2PIN



CPU_MH_M1



YJUMPER-M



X_YJUMPER-M



X_YJUMPER-M